

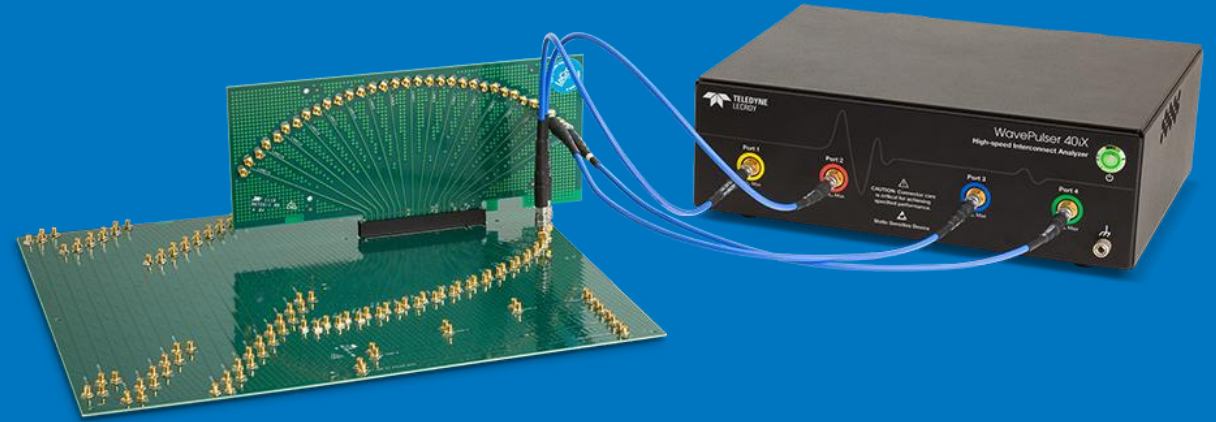
WavePulser 40iX

Time-Domain Techniques for De-embedding and Impedance Peeling

High Speed Interconnect Analyzer

April-2020

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**Unmatched
Characterization
Insight**

WavePulser 40iX: Testing in frequency and time domain

Time Domain

TDR

Frequency Domain

VNA



Deep Toolbox

(S-parameter de-embedding, Time Gating, Emulation equalized eye-diagram and jitter analysis)

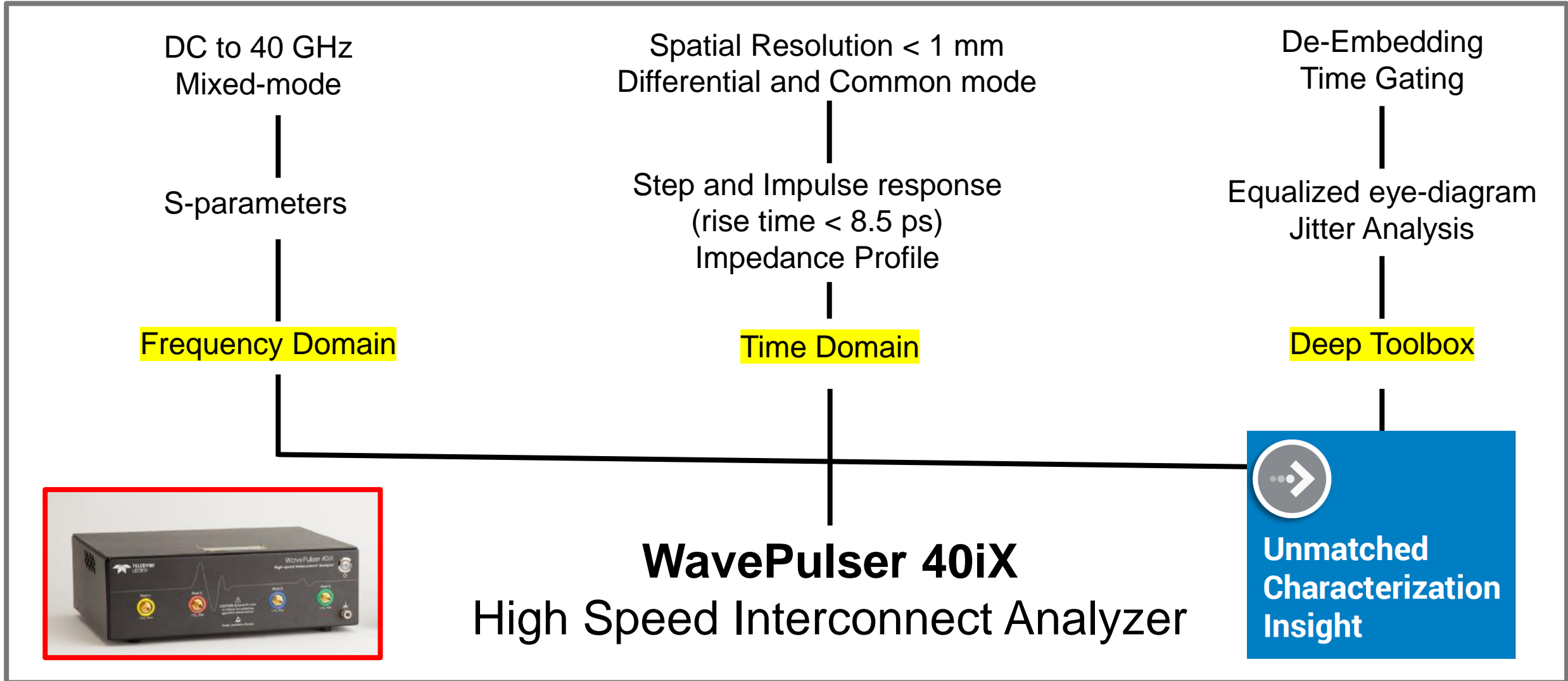
The combination of S-parameters (frequency domain) and Impedance Profile (time domain) **in a single acquisition** with a deep toolbox for simulation, emulation, de-embedding and time-gating provides:



Unmatched
Characterization
Insight

WavePulser 40iX in a nutshell

Testing in frequency and time in a single acquisition



WavePulser 40iX Time-Domain Techniques for De-embedding

- ❑ When measuring S-parameters the DUT is rarely connected directly to the measurement instrument.
- ❑ Generally extra circuitry exists between the DUT and the instrument. Examples are cables, adapters and test fixtures.

❑ De-embedding is the act of removing the extra circuitry surrounding the DUT that is only present for the purpose of making the measurement.

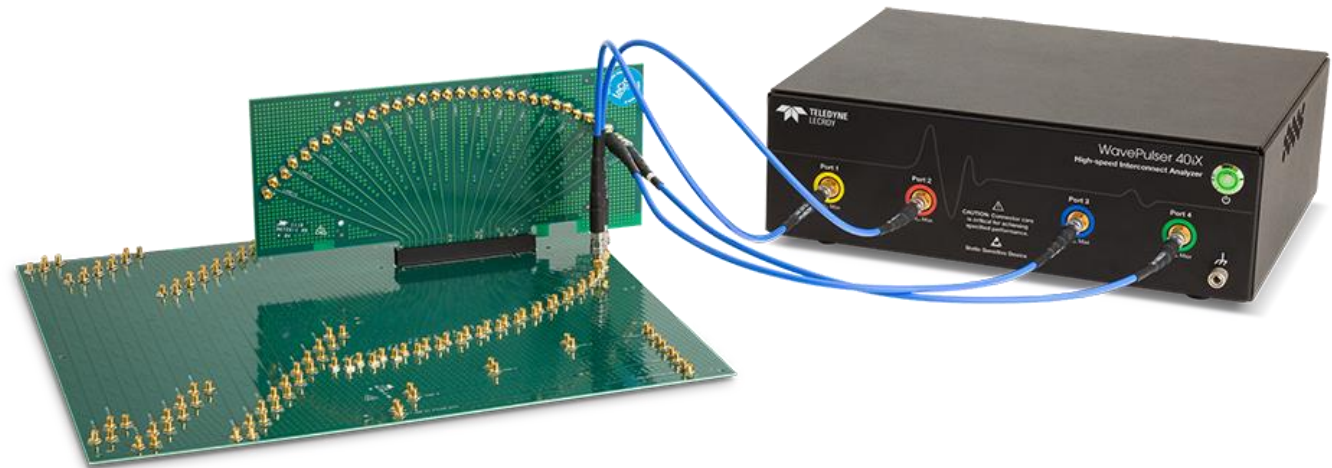
❑ WavePulser 40iX has three methods of de-embedding:

- 1- Calibration methods
- 2- Time-domain methods
- 3- Traditional frequency-domain methods

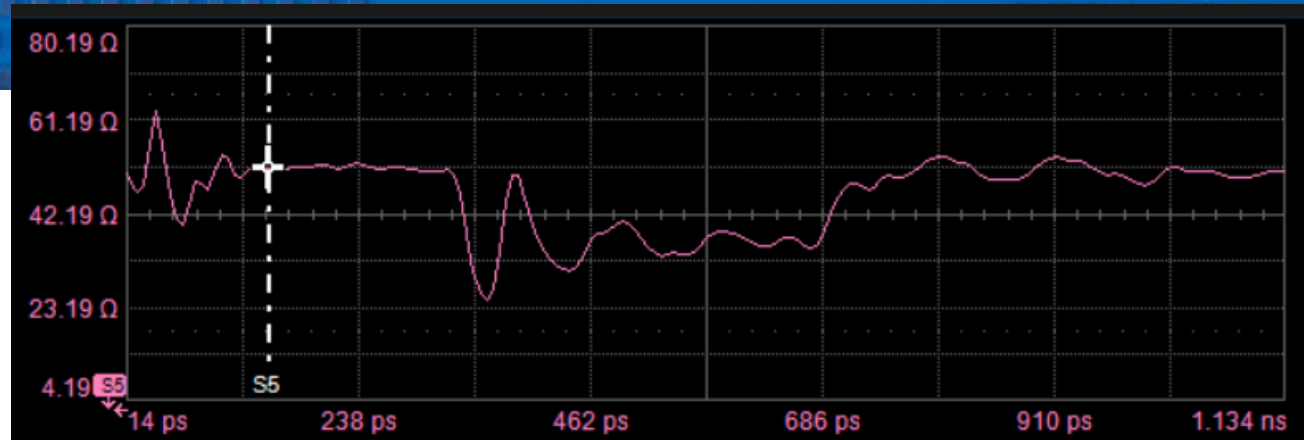
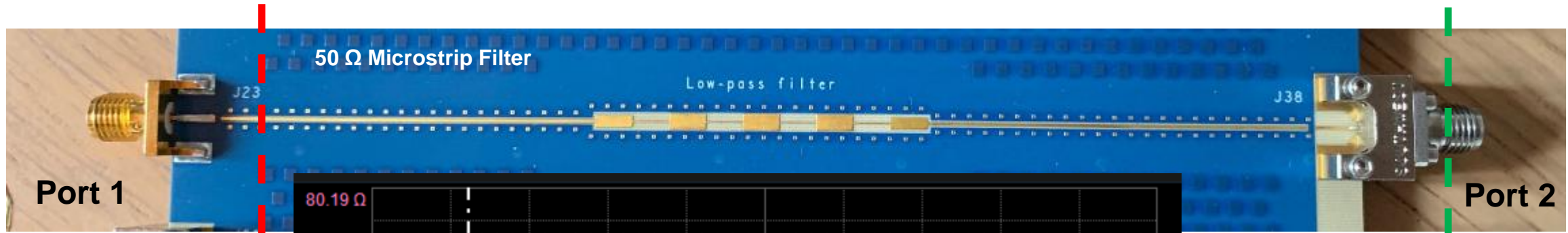
❑ WavePulser 40iX time-domain techniques for de-embedding include:

- ❑ Time Gating
- ❑ Impedance Peeling

High-speed Interconnect Analyzer: the ideal single tool for high-speed hardware designers and test engineers



WavePulser 40iX time gating



The touchstone file for the de-embedded device can be found in C:\LeCroy\Wavepulser\Gating

- Name
- ★ GatingElement_1.s2p
- ★ GatingElement_2.s2p
- ★ GatingElement_3.s2p
- ★ GatingElement_4.s2p

The simplest form of time-domain de-embedding is time gating:

- ❑ A 50 Ω section of transmission line with a specific electrical length is de-embedded
- ❑ It can be used for well-matched, low-loss adapters with an amount of electrical length
- ❑ Predetermined value of Loss can be entered

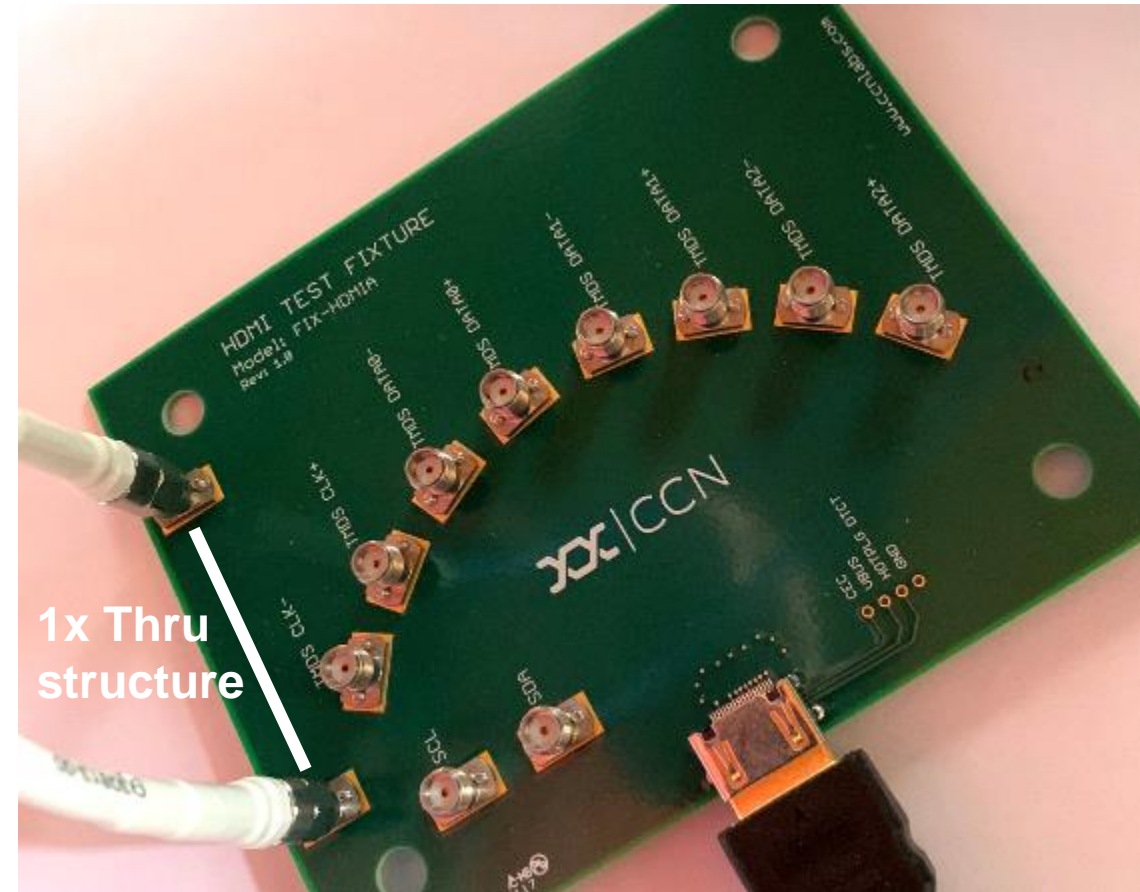
Enable Gating element s-parameter files will be written to: C:\LeCroy\WavePulser\Gating\

User Port	Enable	Peeling	Z	Delay	Loss
Port 1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	152.0 ps	0 mdB
Port 2	<input type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	0.0 ps	0 mdB
unused	<input type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	0.0 ps	0 mdB
unused	<input type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	0.0 ps	0 mdB

Linear loss are defined in dB/GHz/ns

WavePulser 40iX Impedance Peeling

- While time gating is a very simple form of de-embedding used mostly to account for time delay (or electrical length), a improvement can be made by measuring and **accounting for the actual impedance of the line**, even as the impedance changes over the time
- This can be performed automatically and is known as **Impedance Peeling**
 - The **1x thru structure** is a calibration element built onto the test fixture and is intended to be representative of the trace from an SMA connector to the DUT on the fixture.
 - User measures this trace and then de-embed this measurement from the measurements of the DUT.
 - We will de-embed both SMAs using impedance peeling



HDMI test fixture with multiple lanes of measurement along with a 1x thru de-embedding structure (courtesy from CCN, www.ccnlabs.com)

1 x Thru Structure

Return loss (s_{11}) measurement shows the trace is somewhat non-ideal

Insertion loss (s_{21}) measurement shows the trace has 6 dB of loss @20 GHz

Impedance profile shows impedance bounces between 51 Ω and 48 Ω for the first few points (connector on port 1) and then jump to approx. 53 Ω until about 400ps when the connector on port 2 is encountered



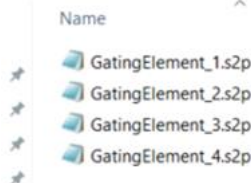
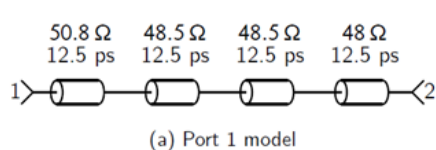
Impedance peeling de-embedding

- ❑ The sample period for the impedance profile plot is **12.5 ps per point**
- ❑ S-parameter measurements from DC to 20 GHz, so sample rate in time domain is 40 GS/s and the sample period 25 ps and 12.5 ps for the impedance profile.
- ❑ There are **four impedance points** for the connectors accounting for **50 ps of electrical length**
- ❑ Apply loss of the measured trace over the connectors as well (dB/GHz/ns)
 $6\text{dB}/20\text{GHz}/0.442\text{ns} = 667.5\text{ mdB}$

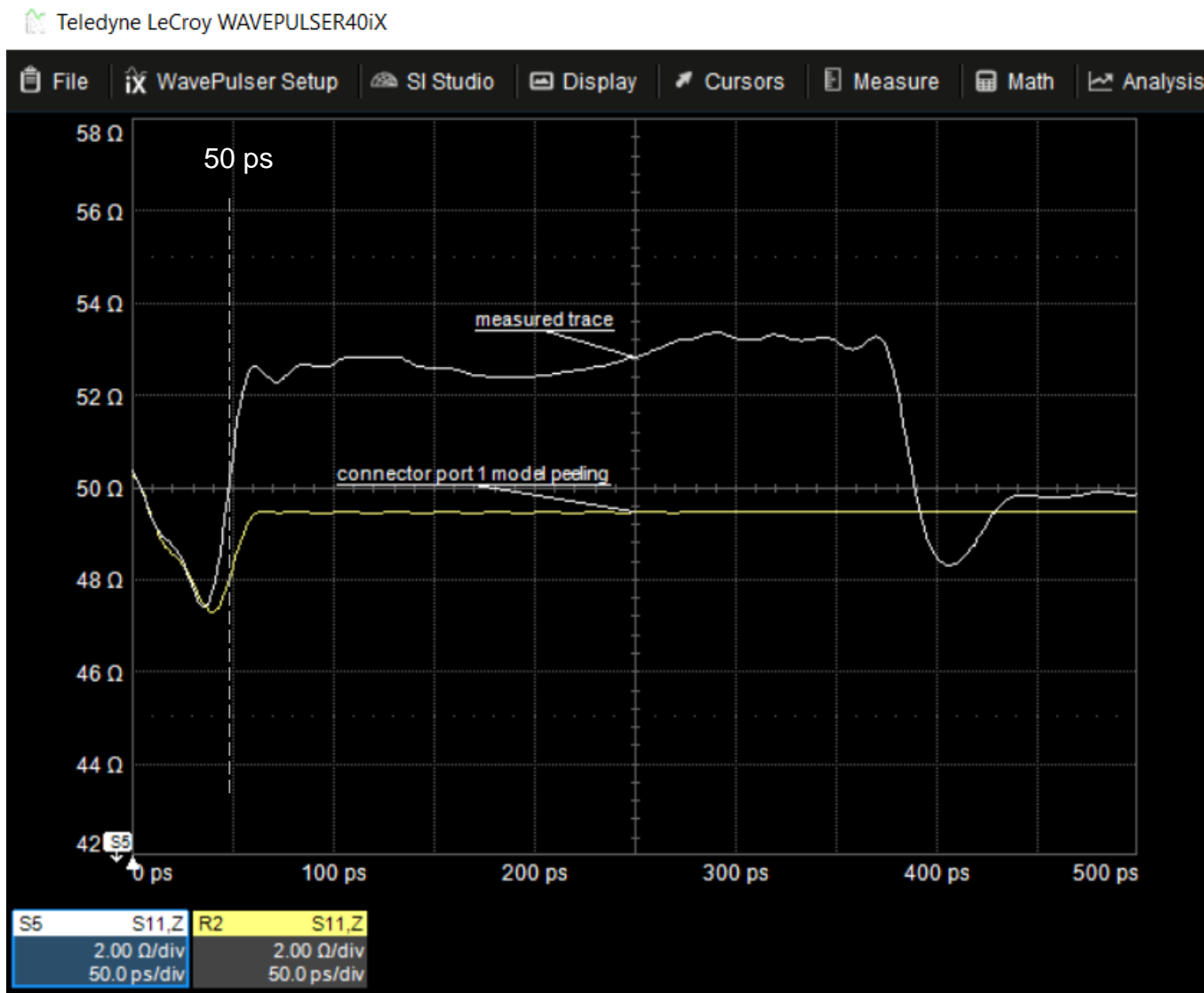


Understand Impedance peeling

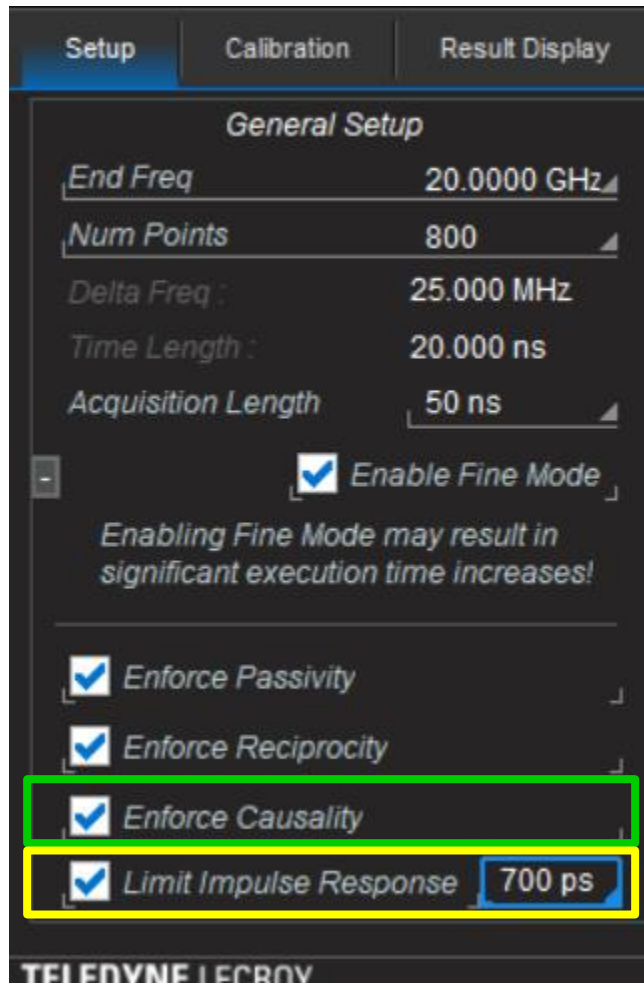
- S-parameter measurements of the peeled structure are available on the directory C:\LeCroy\Wavepulser\Gating



- See the similarity between the impedance profile of the peeled structure port 1 connector to the first 50 ps of the impedance profile of the measured trace



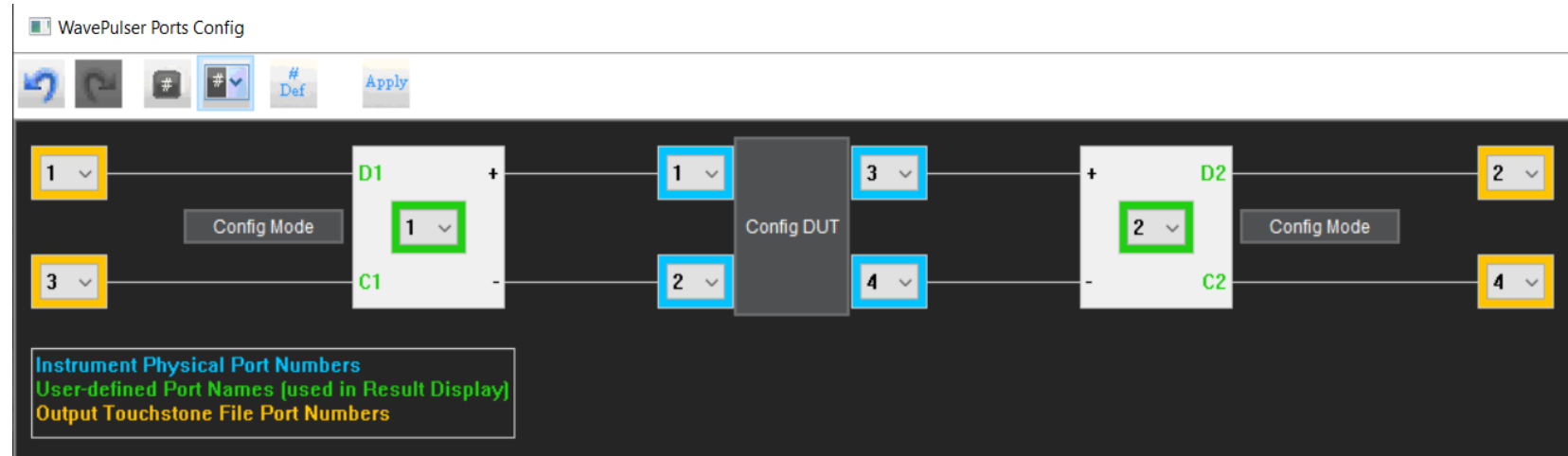
WavePulser 40iX causality enforcement



- ❑ Causality violations are when effects occur prior to time zero and are best viewed and most obvious in the time domain
- ❑ Causality violations are evidence of imperfect de-embedding when the structure being de-embedded. For this reason after time gating and impedance peeling, or any de-embedding, it is advisable to enforce causality on the results
- ❑ To limit the impulse response length is a trick that can be applied by the effect of de-embedding the opposite connectors. In this example if the trace ends at 350 ps, the impulse response length can be limited to 700 ps, taking into account that the incident wave go up and back down the line to form the impedance profile plot

Impedance peeling and coupled lines

- ❑ **Mixed-mode** S-parameter conversion setup is the way to deal with time gating and impedance peeling with coupled lines
- ❑ In a balance configuration the differential transmission line transmits the differential and common-mode with no interactions between the modes. This means that it is possible to measure:
 - ❑ differential-mode impedance profile
 - ❑ common-mode impedance profile



WavePulser 40iX mixed-mode s-parameter conversion setup

WavePulser 40iX time gating menu with mixed-mode measurements

Setup	Calibration	Result Display	TDR/TDT	Result Actions	Instrument Setup	SParam
<input type="checkbox"/> Enable Gating element s-parameter files will be written to: C:\LeCroy\WavePulser\Gating\						
User Port	Enable	Peeling	Z	Delay	Loss	
Port D1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	50.0 Ω	50.0 ps	0 mdB	
Port D2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	50.0 Ω	50.0 ps	0 mdB	
Port C1	<input type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	0.0 ps	0 mdB	
Port C2	<input type="checkbox"/>	<input type="checkbox"/>	50.0 Ω	0.0 ps	0 mdB	

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- ❑ When measuring mixed-mode s-parameter the gating menu shows the **mixed-mode ports for gating**
- ❑ Times for the differential and common modes are different, due to the **different propagation velocities** of the different modes

WavePulser 40iX Time-Domain Techniques for De-embedding



- Time gating and impedance peeling has been seen to be useful de-embedding techniques that are easily performed with the WavePulser 40iX
- A useful aspect of this techniques is its use of the impedance profile measured directly with the WavePulser 40iX
- Causality and impulse response time limiting have been shown to be effective in resolving any small errors created by de-embedding

To know more go to:

<https://teledynelecroy.com/doc/time-domain-de-embedding-and-peeling>

Time-Domain Techniques for De-embedding and Impedance Peeling

TECHNICAL BRIEF

Peter J. Pupalaikis
April 7, 2020

Summary

This brief explains time-domain techniques for de-embedding that are available within the WavePulser40iX called *time gating* and *impedance peeling*.

In addition, methods of using these time-domain techniques with coupled lines are explored.

Introduction

De-embedding is a common problem in making signal integrity measurements because often, the interconnection between the measurement instrument and the device under test (DUT) requires fixtures, cables, and/or probes. While usually it is not too much of a problem to calibrate the instrument to the end of the cables, which present a coaxial connector as the instrument port, the removal of what is between the instrument port and the desired reference plane of the DUT can prove problematic.

Many techniques are possible within the WavePulser40iX for de-embedding such as calibration, and adapter and fixture de-embedding. These techniques are well known by engineers who are familiar with microwave measurements and the vector network analyzer (VNA).

Less well known are time-domain techniques that are available in the WavePulser. These techniques are related to *port extension* employed in the VNA. These time-domain techniques will be described subsequently.

Adapter De-embedding

Many de-embedding applications involve the assumption that there is a two-port device (adapter) connected between one or more ports of the measurement instrument and the ports of the DUT [1]. Figure 1 shows the de-embedding problem posed for a two-port measurement, where the problem is stated as:

Given the known *s*-parameters of a system consisting of a left and right adapter connected to ports 1 and 2, respectively, each connected to the DUT, where the *s*-parameters of the adapters are known, what are the *s*-parameters of the DUT?

This problem has a relatively easy solution, but it requires information that is sometimes the most difficult to obtain – what are the *s*-parameters of the adapters? If the adapter is a coaxial device, like a bullet, this is easily obtained through measurement of the device. This paper concerns itself with de-embedding problems where one side of the adapter is not coaxial, for which a direct measurement of the *s*-parameters is difficult or impossible to obtain.

Time Gating

De-embedding is not a panacea. Usually, when connecting between instrument ports and the DUT, the desire is to have as transparent a connection as possible. This means a characteristic impedance as close to 50Ω as

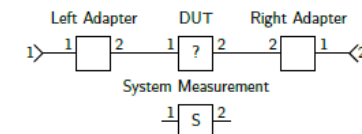


Figure 1: Adapter de-embedding