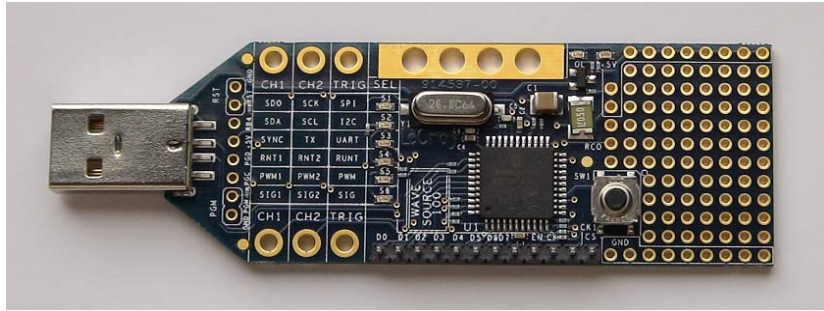
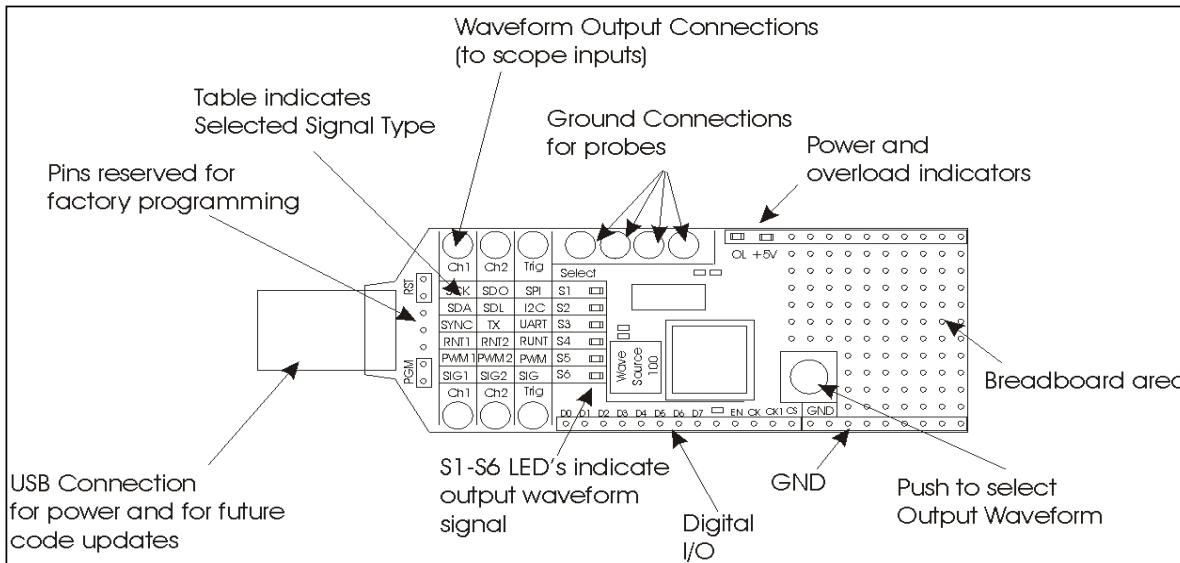


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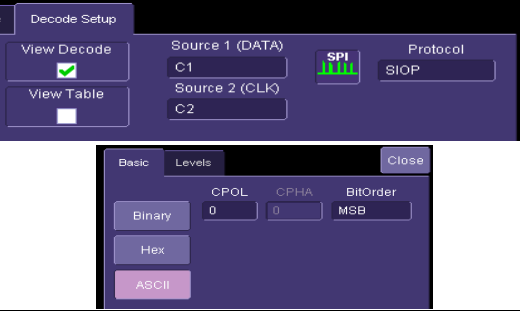
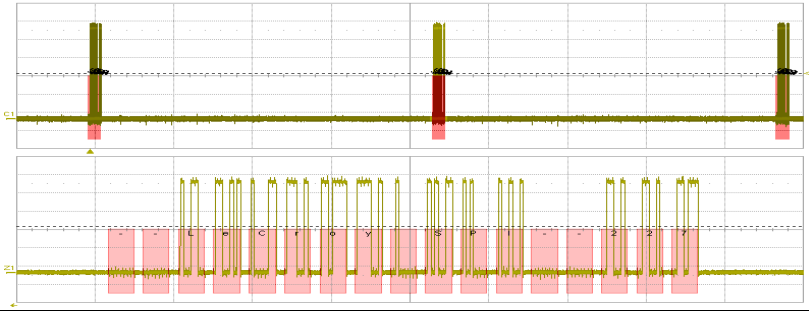
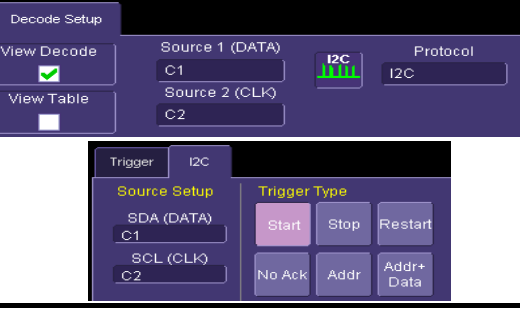
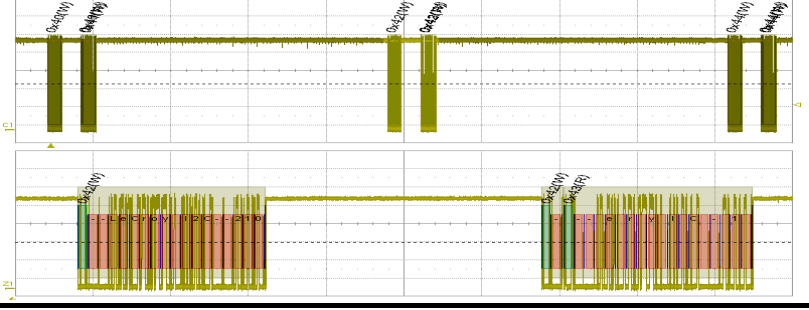
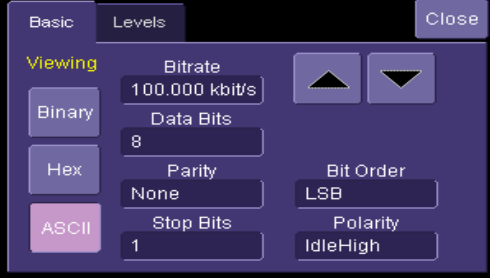
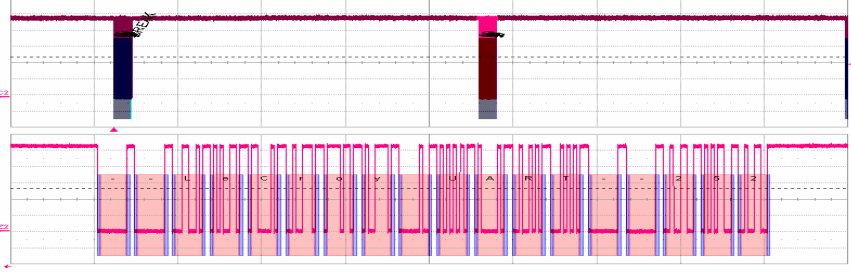
SIGNAL OUTPUTS

SIGNAL	PROTOCOL	CHANNEL 1	CHANNEL 2
S1	SPI	DATA (SDO)	CLOCK (SCK)
S2	I2C	DATA (SDA)	CLOCK (SCL)
S3	UART	Not Used	TRANSMIT (100 kbits/sec)
S4	RUNT	RUNT (positive) JITTER (35%)	RISE TIME (slow = 100 nsec) GLITCH (pos. width = 165 nsec) JITTER (35%)
S5	PWM	PERSISTENCE (9 pulse widths incrementing in width and quantity)	LONG MEMORY (500 KHz and 750 KHz, 33 msec delay)
S6	SIG	Not Used	NON MONOTONIC Edge RUNT (negative)

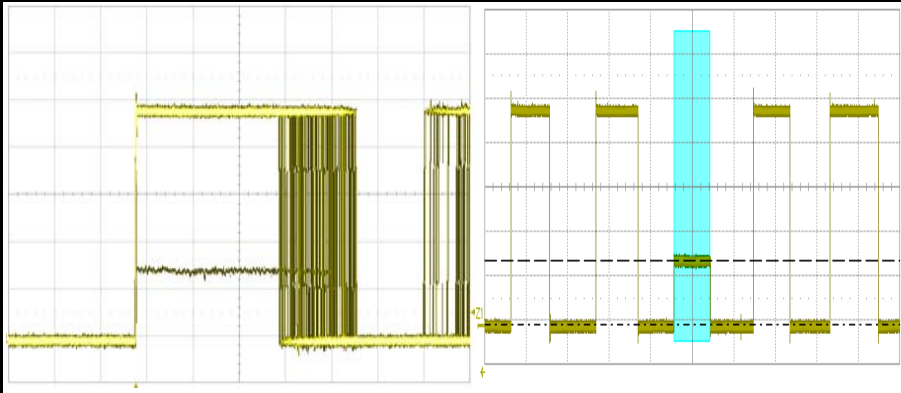
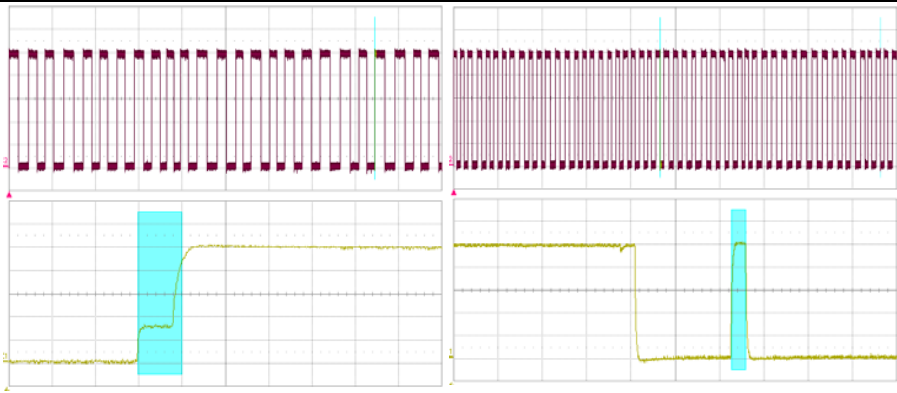
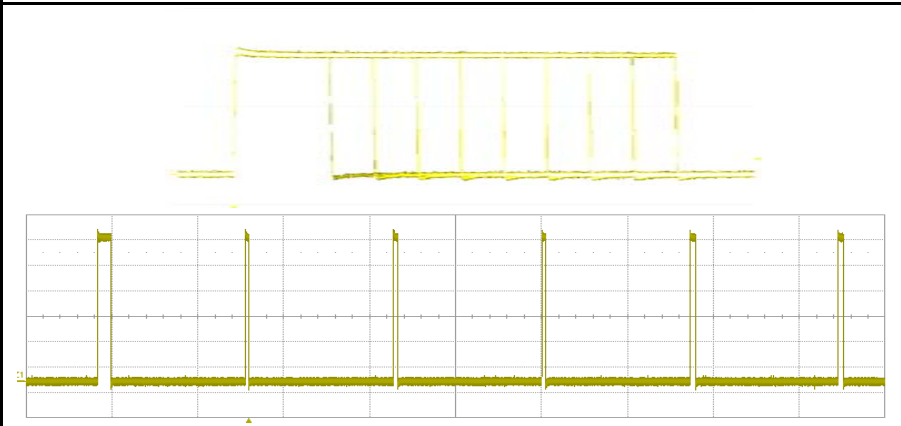
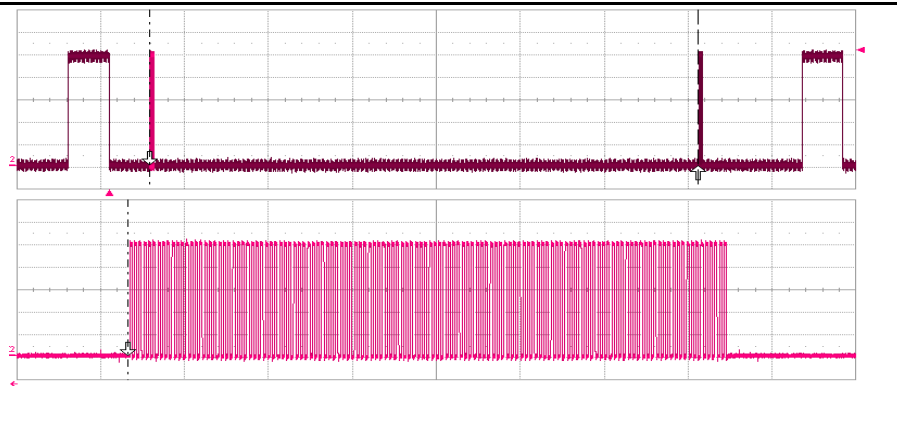


Steve Murphy
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SIGNAL PROTOCOL	OUTPUT SIGNALS		OUTPUT AND SCOPE SETUP SUMMARY
	CHANNEL 1	CHANNEL 2	
S1 SPI	SDO DATA	SCK CLOCK	<p>Bit Rate=100 kbit/s, CPOL= CPHA=0, Bit Order= MSB, Message= "LeCroy SPI <cnt>", repeat rate= 44ms, idle low, cnt= 1 to 3 digits, 0 to 255</p> 
			
S2 I2C	SDA DATA	SCL CLOCK	<p>Bit Rate= 100 kbps, Message= "LeCroy I2C <cnt>", repeat rate= 44ms, idle high. 25-byte long frame every 61 messages. 10-bit address every few messages. Incrementing address from 10h to 2Fh. Write frame followed with Read frame.</p> 
			
S3 UART	Not Used	TRANSMIT	<p>Bit Rate= 100 kbit/s, Data Bits= 8, Parity= NONE, Stop Bits= 1, Bit Order= LSB, Polarity= IdleHigh, Message= "LeCroy UART <cnt>". Repeat rate = 44ms. Break sent at end of every few messages.</p> 
			

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SIGNAL PROTOCOL	OUTPUT SIGNALS	
	CHANNEL 1	CHANNEL 2
S4 RUNT	<p>JITTER (35%) RUNT (positive)</p> 	<p>RISE TIME (slow=105 nsec) WIDTH (pos.glitch = 165 nsec) JITTER (35%)</p> 
	<p>Both outputs are 5 V square waves with freq.= 2.0-3.2 KHz and jitter = 35%; Channel 1: has positive runt (1/3 height) occurs every 200 msec. or 1:500 pulses; Channel 2: Risetimes averaging 26-35 nsec. with a slow rise of 105 nsec. every 200 usec. or 1:500 pulses; Widths range 152-240 usec. with a narrow glitch of 165 nsec. occurring 3 and 51 edges before the glitch (10 msec's apart and repeating every 200 msec.)</p>	
S5 PWM	<p>PERSISTENCE TRACE (incrementally repeating pulse width pattern)</p> 	<p>LONG MEMORY TRACE (short bursts of 500 KHz and 750 KHz square waves separated by long delay)</p> 
	<p>Channel 1: 5V positive pulse width pattern starts from single pulse of 1.66 usec. width, linearly increases number of pulses for each increasing value of pulse widths. Widths increment in 0.75 usec steps, i.e.. 2 pulses at 2.41 usec., 3 pulses at 3.16 usec. until reach 9 pulses at 7.66 usec. widths. Repeats every 86 usec. Channel 2: 5V 500 KHz and 750 KHz bursts of 127 cycles each, starting 33 msec. apart. Effectively short bursts separated by long delay. This repeating output is preceded by positive 2.4 usec. pulse and 2.4 usec. delay. Repeats complete pattern every 44 msec.</p>	

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SIGNAL PROTOCOL	OUTPUT SIGNALS	
	CHANNEL 1	CHANNEL 2
S6 SIG	Not Used	NON MONOTONIC Edge RUNT (negative)
<p>Channel 2 only: 3V square wave that has a non-monotonic edge (starts at 1.8V from ground on the positive slope, drops 1.25 V before transitioning to the high level. Signal also contains a negative runt on the top of a positive pulse. This is 1.5 KHz signal with the negative runt and non onotonic edge occuring every 680 msec.or 1:1,000 pulses.</p>		

DIGITAL OUTPUTS	
	<p>8 Parallel digital ouputs always available at the Digital I/O connector, 40 KHz clock.</p>