LeCroy

CIS Timebase Operation

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The WaveExpert CIS timebase has a maximum record size of 512 MS and an almost fixed sample rate of 10 MS/s. The timebase is not triggered but requires an external clock that is synchronized to the input waveform. Clock frequencies between 125 MHz and 13.5 GHz must be connected to the prescaler input and clock frequencies between 62.5 MHz and 125 MHz must be connected to the trigger input. The CIS timebase will not accept clocks below 62.5 MHz.

The CIS timebase uses a phase locked loop (PLL) to synchronize an internal clock of about 2.56 GHz to the external clock input. However the synchronization is not exact. It differs from the external clock by a known amount based on an algorithm that sets the appropriate fractional dividers in the PLL. An additional **Divide By** 256 generates an approximate 10 MHz strobe from the internal 2.56 GHz clock. This strobe drives a sampler that samples the input waveform at the computed approximately 10 MS/s. The time between samples is about 100 ns. Many cycles of the input waveform will pass between samples. No trigger is required, once the timebase is synchronized to the external clock, as many samples may be acquired as desired at the approximately 10 MS/s rate. Note that 4 MS will be acquired in 0.4 seconds.

Several control inputs are needed by the CIS timebase **Bit Rate**, **PLL Bandwidth**, **Pattern Length**, **Samples/UI**, and **Ext. Divider**.

Bit Rate

The **Bit Rate** control **must** be set to the bit rate or frequency of the pattern even if the pattern is as simple as a sine wave or square wave. Here is an example of a 10 GHz sine wave when the bit rate is set to 9 GHz instead of 10 GHz. The display is not recognizable as a pattern.

Note that the out of lock indicator in the horizontal descriptor box is red, indicating the input clock rate is not the same as the Bit Rate. As a user of the oscilloscope you will have to enter the bit rate or frequency of the input signal in the **Bit Rate** control box.

PLL Bandwidth

The CIS timebase has a PLL to synchronize the strobe out-put to the clock input. The PLL has two bandwidth settings Low and High corresponding to about 10 kHz and 1 MHz respectively. These are set with the **PLL Bandwidth** control. The CIS timebase has the lowest time jitter on the Low setting. If you want to measure all the jitter on the signal input above 10 kHz, then use the Low setting. Any jitter between DC and 10 kHz will be tracked by the PLL and will not appear on the measured signal. If you want to mea-sure all the jitter on the signal input above 1 MHz and track the jitter from DC to 1 MHz, then use the High setting.

Pattern Length

The pattern length of the signal can be selected by setting Custom in the Std. Pattern selection box or picking one of the many standards available.

Shown below are PRBS7 and a pattern length of 127. CIS has the remark-able ability to display a pseudorandom pattern signal source without a trigger source. Here is a screen shot of a portion of a 2 Gbit/s pseudorandom pattern that is 127 bits or 2^7-1 bits long.

Any pattern length up to 2^31 –1 or 2147483647 bits long can be acquired with certain restrictions.

Samples/UI

The number of samples per bit period or unit interval, UI, can be changed with the **Sample Density** control. Here is the same signal as above at 8 S/UI.

Notice that the horizontal position in the pattern is not the same as in the first screen shot. When the sample density was changed, the internal PLL was reprogrammed which changed the phase of the internal 2.56 GHz clock with respect to the external 2 GHz clock. The result is an unknown start phase for the pattern. As long as **Sample Density** and **Bit Rate** are not change or the external signal is not change the phase will remain the same.

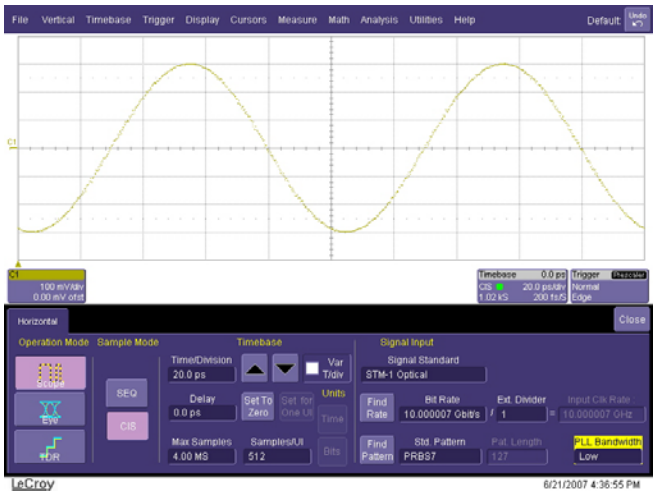
Ext. Divider

Some pattern generators have an output clock that is a divided clock from the bit rate of the pattern. That division ratio can be set with this control. Notice in the above screen shot that the **Ext. Divider** control is followed by an input clock rate indicator showing the actual clock input to the sampling scope.

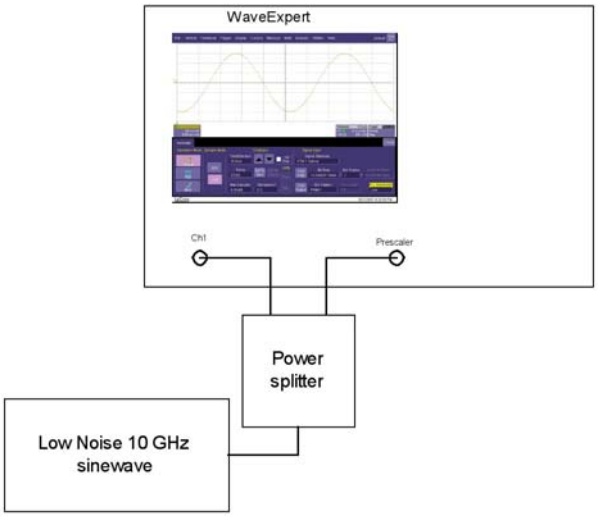
CIS Jitter

The CIS timebase has less than 250 fs rms of time jitter. This can only be measured with a low jitter signal source that has a large enough amplitude and a high enough frequency to ensure vertical noise is not a contributor to the jitter. We measure the jitter with a 10 GHz sine wave at about 6 dBm amplitude. The signal source is a sine wave from an Anritsu synthesized signal source. The estimated jitter of this signal source is less than 150 fs rms.

Here is a screen shot of a 10 GHz sine wave acquired by the CIS timebase.



Below is one technique to measure the jitter of the CIS timebase. Connect the scope to a low noise sine wave source. Here is the setup to use.



Setup the scope in the following fashion (see the screen shot below). Set F1 = C1, F2 = eres(F1)-F1 and F4 = eres(F1). Eres is set to 3 in both math functions. Using F1 = C1 allows one to easily change the measurement channel by changing the source of F1.

Math function F2 smoothes the sine wave removing the noise then subtracts the original sine wave leaving just the noise. Notice the pink F2 trace on the screen below showing the noise at the zero crossing and very little noise at the peaks of the sine wave. Parameter P1 measures the standard deviation of the noise in the middle of the screen on F2. The right and left gates of P1 were moved in to the middle of the screen within ±0.2 division.

Parameter P2 measures the slew rate of the smoothed sinewave in math function F4. The right and left gates of P2 were moved close to the middle of the screen to measure the slew rate of the same edge that is measured.

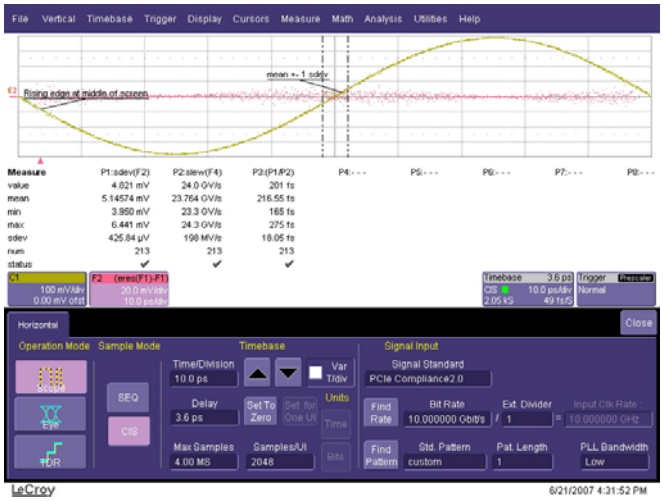
P3 uses parameter math to take the ratio of the P1 and P2 to calculate the rms jitter.

The voltage noise of the sampler has to be taken into account when the signal amplitude is small. For example in the above setup the voltage noise of the sampler is about 0.7 mV rms. Subtracting this in quadrature from the measured sdev of F2 gives an actual sdev value of:

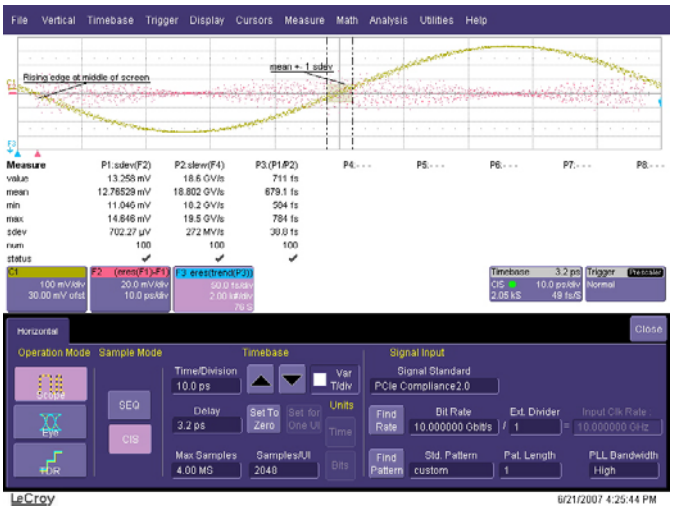
Actual sdev = sqrt(5.14574^2-0.7^2)=5.098 mV rms.

This changes the jitter from 216.55 fs to 214.5 fs, a minor adjustment to the jitter. However, if the amplitude of the sine wave is reduced, the measured sdev at the zero crossing will decrease and now the 0.7 mV rms voltage noise of the sampler module will become more important. The same thing happens if you reduce the frequency of the sine wave; the slew rate decreases so the sdev of the noise at the zero crossing decreases again.

If you use a higher bandwidth sampler the voltage noise will be larger and you may have to take it into account when you measure the jitter with the above technique even with the same amplitude.



Below is the same setup with the PLL Bandwidth set to High.



The added jitter is due to the jitter of the signal source added in quadrature to the jitter of the timebase from DC to 1 MHz. The time jitter is easily visible at the zero crossing of the sine wave. Notice again that there is very little noise at the peaks of the sine wave showing low vertical noise due to the signal source and sampling module.