SDA-HDMI

Software Option

Rev 1.2a

New Compliance Framework

HDMI™
HIGH-DEFINITION MULTIMEDIA INTERFACE

Featuring LeCroy's

Operator's Manual

September 2006

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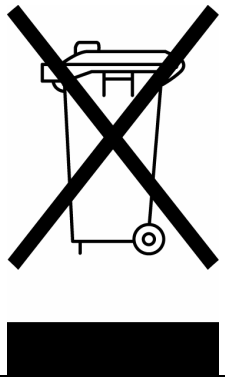

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INTRODUCTION TO HDMI

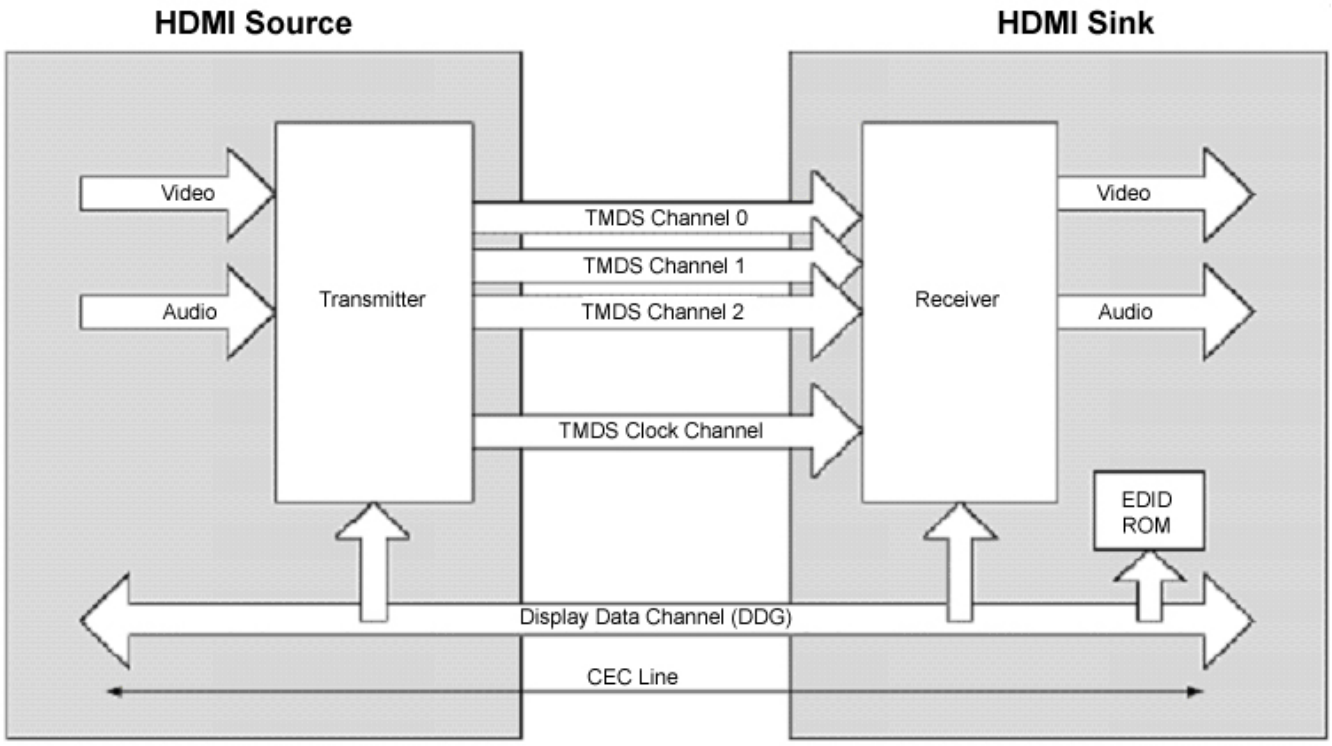
Developed by Sony, Hitachi, Thomson (RCA), Philips, Matsushita (Panasonic), Toshiba, and Silicon Image, the High-Definition Multimedia Interface (HDMI) has emerged as the connection standard for HDTV and the consumer electronics market. HDMI is the first and only digital interface to combine uncompressed high-definition video, multi-channel audio and intelligent format and command data in a single digital interface. For end-users, use of a single cable for audio and video dramatically simplifies home theater system installation by eliminating the tangle of cables typically associated with home theater system components.

Most importantly, HDMI offers significant advantages over analog A/V connections, including the ability to transmit uncompressed digital video and audio content. And INTEL allows use of its proprietary High Definition Content Protection (HDCP) scheme for DVI and HDMI, perhaps the best solution for the digital video interface, which transfers high definition video content and is easy to implement.

Since the Digital Display Working Group (DDWG), the standards body that specifies DVI, decided to focus on the computing market, the HDMI working group has taken over the role in consumer electronics. In addition to numerous device and display manufacturers, Hollywood studios and cable and satellite operators also support HDMI.

Key Specifications and Product Features

HDMI system architecture is defined as consisting of Sources, Sinks, Repeaters, and Cable Assemblies. A given device may have one or more HDMI inputs, and one or more HDMI outputs.



HDMI Block Diagram

Each HDMI input on a device follows all of the rules for an HDMI Sink, and each HDMI output follows all of the rules for an HDMI Source. Consequently, each HDMI input is fully tested for compliance using the tests specified for Sink devices, and each HDMI output is fully tested against the full set of tests specified for Source devices.

Engineering Tasks

Required Test Equipment Capabilities

- The Jitter/Eye Analyzer must be capable of accurately indicating the amount of jitter, or the actual eye diagram, on the tested transition minimized differential signal (TMDS).
- The transfer function for an ideal recovery clock is given by Equation 4-1 from HDMI Specification 1.0a and 1.2a, shown below. An ideal clock recovery unit (CRU) would perfectly match this function.
- Across the tested clock frequency range, the Jitter/Eye Analyzer's CRU shall have a jitter transfer amplitude that differs from the ideal transfer function by no more than ±0.2 dB from DC to10 MHz. At 20 MHz the difference must be less than ±1 dB, and at 50 MHz, less than +2/-6 dB. From DC to 20 MHz, the jitter transfer phase response must be within ±1.8 degrees of the phase response of the ideal recovery clock.

$$H(j\omega) = 1/(1 + j\omega/\omega_0) \qquad \text{(Eq. 4-1)}$$

where $\omega_0 = 2\pi f_0$, $f_0 = 4.0$ MHz

INTRODUCTION TO SDA-HDMI

The LeCroy HDMI Compliance Test Software for the SDA4000A, SDA4020A, SDA5000A, SDA6000A, SDA6020 and SDA11000 serial data analyzers is designed with the following major objective in mind:

> SDA-HDMI provides the necessary tools to develop HDMI compliant source devices in a systematic, step-by-step fashion, in accordance with the latest standards and specification documents published by HDMI founders.

The standard features of the SDA also provide a broad tool set for advanced debugging of these interfaces, including jitter, eye pattern, and bit error rate.

The LeCroy HDMI Compliance Software (SDA-HDMI) can work with version 4.6.3 or later of X-Stream DSO firmware.

Required Equipment

- SDA 4000A, SDA 4020A, SDA 5000A, SDA 6000A, SDA 6020 or SDA 11000 (16 Mpts memory per channel)
- HDMI Compliance Test software option (LeCroy SDA-HDMI)
- 2 differential probes (D350 type)
- 1 set of compliance test fixtures (TF-HDMI: TPA-P-DI and TPA-P-SE)
- A host computer, though not required, is highly recommended to execute X-Replay, the compliance & development software engine.
- 3.3 V power supply
- EDID interface or means to control the interface

HDMI Compliance Test Fixtures

The HDMI standard describes a set of two fixtures that are used to connect to the signal under test. The fixtures are known as the TPA-P-DI and the TPA-P-SE. The TPA-P-DI is used to test the signal as a differential input, and the TPA-P-SE is used to test the signal as a single-ended input. TPA-P-DI and TPA-P-SE are available from LeCroy as a set, under product code TF-HDMI.

Both fixtures terminate all differential lines with a 50 ohm resister to V_{cc} (3.3 V) on board, and provide probing points for an active probe to pick up the signal.

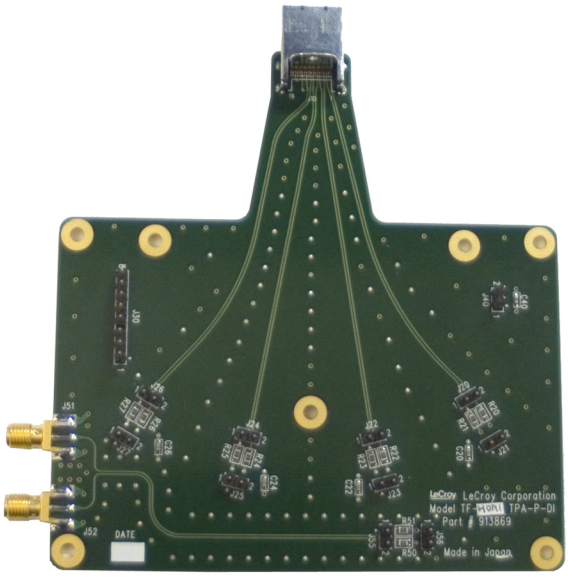


Figure 1. HDMI test fixture TF-HDMI TPA-P-DI provides an HDMI plug connector to connect an HDMI source device. The 3.3 V power supply connection is at the square pin header. All TMDS differential signals, D0, D1, D2, and CLK are picked up from corresponding square pin headers. The EDID emulator is connected to an 8-pin square pin header to communicate with the source device under the test..

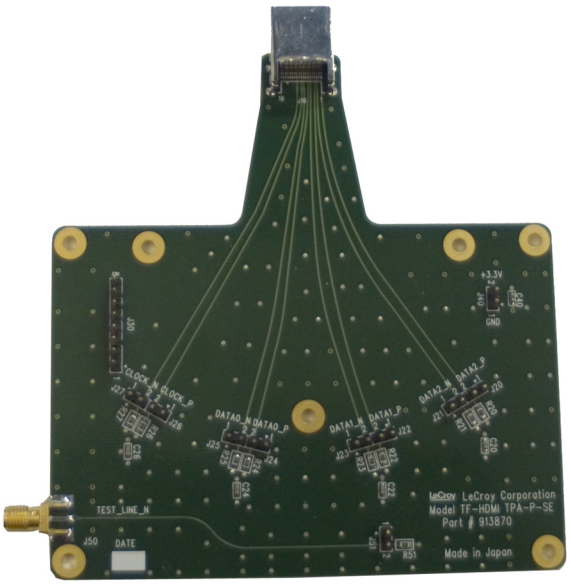


Figure 2. HDMI test fixture TF-HDMI TPA-P-SE is similar to TPA-P-DI but TMDS differential lines are separated as two single-ended lines for the corresponding test.

J30 CONNECTOR	
Pin	**Signal**
8	GND
7	CEC
6	RESERVED
5	DDC_CLK
4	DDC_DATA
3	P5V_GND
2	+5 V
1	Hot_Plug

What Is X-Replay?

The HDMI Compliance Test software application incorporates X-Replay, a unique application framework. X-Replay is an MS Windows-based application that contains all the commands and instructions necessary to configure, acquire, display, and report measurement results. For instance, the X-Replay environment enables you to:

- Create or change test criteria in order to make context-sensitive parametric measurements.
- Export all test results as XML for import into a database program, such as Microsoft Access, for further manipulation.
- Generate reports from within X-Replay, showing the latest test results. Reports are html and are meant to be viewed with Microsoft Internet Explorer.

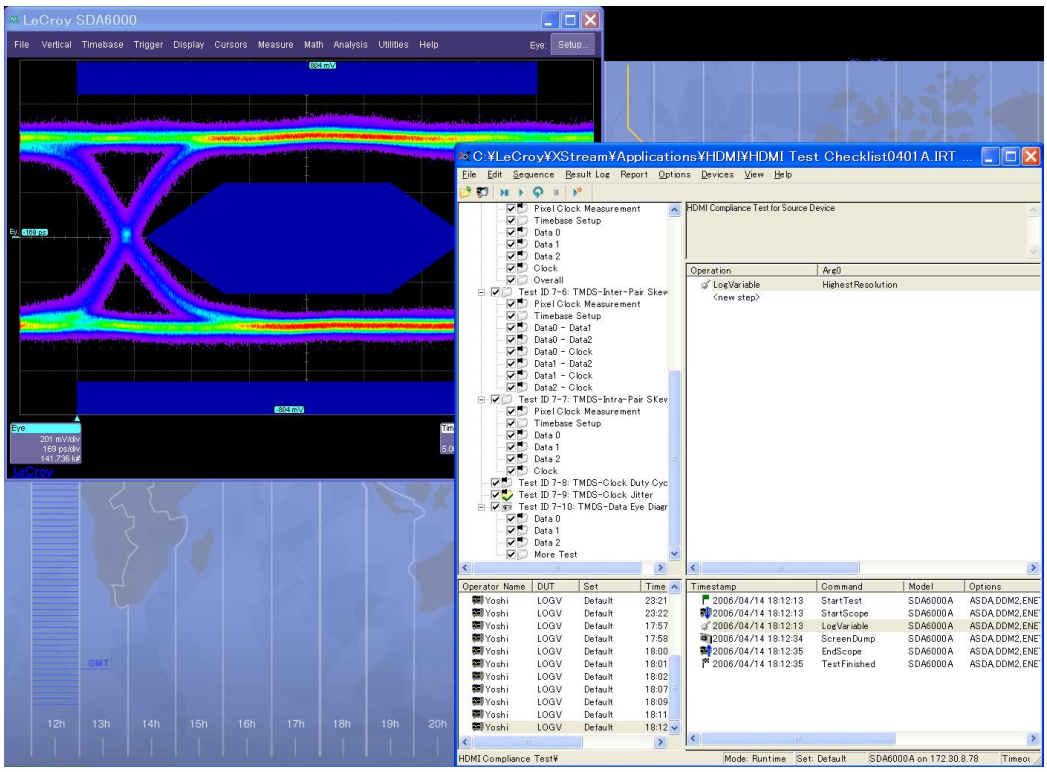


Figure 3. X-Replay Window

The HDMI Compliance Test software resides in X-Stream DSO software in the scope, and it is activated through the use of an alphanumeric code matched to the scope's serial number. Unique to each scope serial number, this code is activated when you order SDA-HDMI software.

While the software key enables the scope to perform the measurements, X-Replay contains the HDMI script, the test results database, and the report generation engine. For ultimate flexibility, X-Replay can be executed from a host computer at a remote location, provided that there is a Windows-compatible network connection.

SOFTWARE INSTALLATION AND SYSTEM CONFIGURATION

Option Key Installation

When ordered as an option for a new instrument, no installation of SDA-HDMI is necessary. Installation is required, however, when the option is ordered after the oscilloscope is purchased. An option key will be issued at the time the option is purchased.

To enter the option key code,

1. Touch **Utilities** in the menu bar, then **Utilities Setup…** in the drop-down menu.
2. Select the “Options” tab from the utilities dialog.
3. In the Options dialog, touch the **Add Key** button and enter the option key in the dialog box, using the on-screen keyboard.

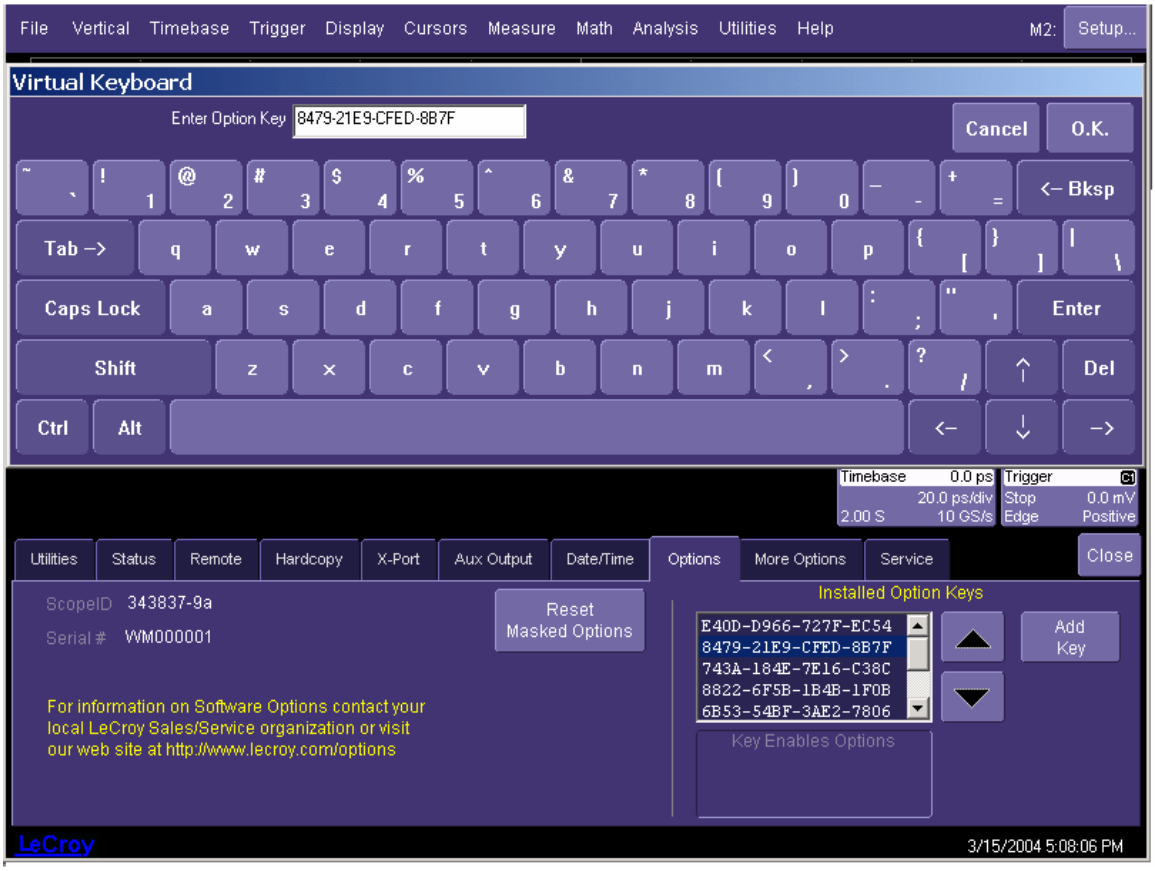


Figure 4. Entering the option key code for the SDA-HDMI software option

CD-ROM Installation

When ordered as an upgrade to an existing X-Stream instrument, an Application Software CD-ROM is supplied containing X-Replay and other software installation files. Follow the specific instructions in the Installer application. When necessary, the installation process will prompt you for storage locations for data files and test results, reports, scripts, etc.

PREPARING TO MAKE HDMI MEASUREMENTS

Channel Deskew (SMA Cables)

HDMI signals are properly probed using two separate channels on the oscilloscope connected to the appropriate SMA jacks on the test fixture. The highest measurement accuracy is achieved when the timing skew between the two channels is calibrated. This is performed using the “Deskew” control on one of the two channels to which the differential signal is connected, as follows:

1. Attach the calibrator signal to both input channels using a “T” connector to rout the calibrator signal on the SDA front panel through the same cables that will be connected to the fixture.

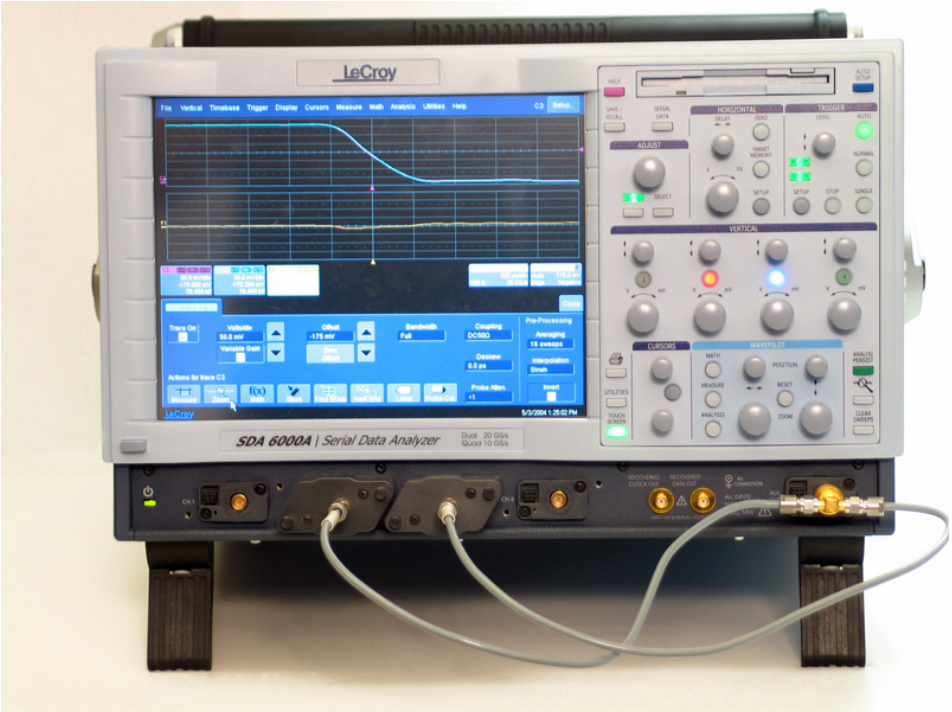


Figure 5. Deskew cable setup. The calibrator signal is connected to the cables using a “T” connector or resistive divider. The calibrator peak voltage should be set to the same value as the nominal voltage of D+ and D-.

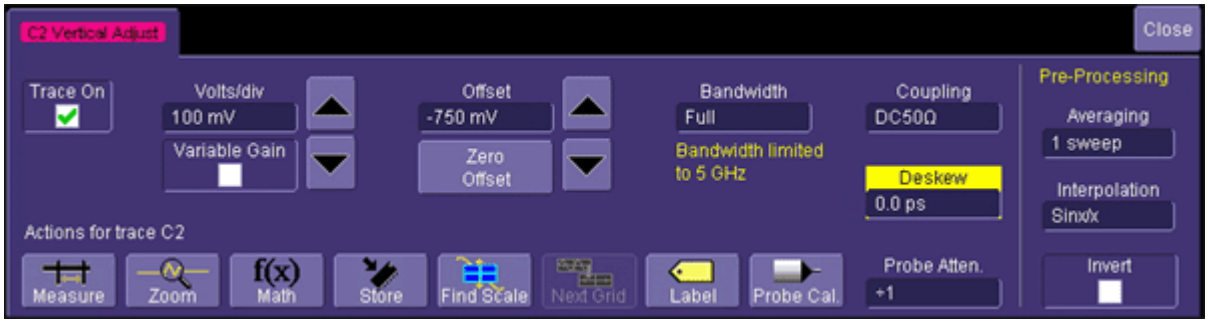


Figure 6. Deskew control in channel menu. Adjust this value to achieve minimum skew.

2. Set interpolation of both channels to **Sinx/x**, using the “Interpolation” control in the “Vertical Adjust” dialog for each channel.
3. Create a Difference math waveform by selecting **Math** in the menu bar, then **Math Setup…** in the drop-down menu. Enter the channels to which your signal is connected in the **Source1** and **Source2** fields, and select **Difference** from the **Operator1** menu. The math function is thus defined as the difference between the 2 channels probing the D^+ and D^- signals.

4. While viewing the math trace, adjust the **Deskew** control in one of the channels until the math trace is as flat as possible.

Note: With the "Deskew" control highlighted, you can use the front panel **ADJUST** knob to make the adjustment.

The best accuracy is achieved by setting the level of the calibrator signal to match the expected levels of the signal under test, and with the calibrator set to its maximum frequency (5 MHz). The calibrator settings can be found in the "Utilities" dialog under the **Aux Output** tab.

Save the deskew value for Channel 2 for use later in the test program

Table 1. Parameter List – Transmitter Compliance Tests (measured at the Tx package pins)

Test ID	Test Name
7-2	TMDS-VL
7-4	TDMS Trise/Tfall
7-5	TMDS Over/Undershoot
7-6	TMDS-InterPair Skew
7-7	TMDS IntraPair Skew
7-8	TMDS Clock Duty Cycle
7-9	TMDS Clock Jitter
7-10	TMDS Data Eye Diagram

Table 2. Test Limits

Name	Comparison Method	Reference
Data0+_TMDS_VL	2.7 < n < 2.9	
Data0-_TMDS-VL	2.7 < n < 2.9	
Data1+_TMDS-VL	2.7 < n < 2.9	
Data1-_TMDS-VL	2.7 < n < 2.9	
Data2+_TMDS-VL	2.7 < n < 2.9	
Data2-_TMDS-VL	2.7 < n < 2.9	
Clock+_TMDS-VL	2.7 < n < 2.9	
Clock-_TMDS-VL	2.7 < n < 2.9	
TMDS-VLmax	2.7 < n < 2.9	
Data0_Trise_Min	>	75
Data0_Trise_Max	<	0.4
Data1_Trise_Min	>	75
Data1_Trise_Max	<	0.4
Data2_Trise_Min	>	75
Data2_Trise_Max	<	0.4
Clock_Trise_Min	>	75
Clock_Trise_Max	<	0.4
Data0_Tfall_Min	>	75
Data0_Tfall_Max	<	0.4
Data1_Tfall_Min	>	75
Data1_Tfall_Max	<	0.4
Data2_Tfall_Min	>	75
Data2_Tfall_Max	<	0.4
Clock_Tfall_Min	>	75
Clock_Tfall_Max	<	0.4

Data0_Overshoot	<	0.15
Data1_Overshoot	<	0.15
Data2_Overshoot	<	0.15
Clock_Overshoot	<	0.15
Max_Overshoot	<	15
Data0_Undershoot	<	0.25
Data1_Undershoot	<	0.25
Data2_Undershoot	<	0.25
Clock_Undershoot	<	0.25
Max_Undershoot	<	25
Inter_Pair_Skew_D0_D1	<	0.2
Inter_Pair_Skew_D0_D2	<	0.2
Inter_Pair_Skew_D0_Ck	<	0.2
Inter_Pair_Skew_D1_D2	<	0.2
Inter_Pair_Skew_D1_Ck	<	0.2
Inter_Pair_Skew_D2_Ck	<	0.2
Data0_Intra_Pair_Skew	<	0.15
Data1_Intra_Pair_Skew	<	0.15
Data2_Intra_Pair_Skew	<	0.15
Clock_Intra_Pair_Skew	<	0.15
Clock_Duty_Cycle	40 < n < 60	
Clock_Jitter	<	0.25
Tbit	>	0
Tbit_Lowest_Frequency	>	0
Tbit_Highest_Frequency	>	0
Data_Eye_Mask_Violation	<=	1
Data_Jitter	<	0.3
Data0_Jitter	<	0.3
Data1_Jitter	<	0.3
Data2_Jitter	<	0.3
Data0_Eye_Violation	<=	1
Data1_Eye_Violation	<=	1
Data2_Eye_Violation	<=	1
Max_Inter_Pair_Skew	<	0.2
Max_Intra_Pair_Skew	<	0.15
MaxDJitter	<	0.3

X-REPLAY CONFIGURATION

Typical Configuration (Recommended)

SDA-HDMI software can be executed from the scope PC or from a Host PC. By default, a new scope will come equipped with X-Replay installed in the scope. LeCroy recommends running SDA-HDMI in a scope equipped with Dual Monitor Display capability (Option DMD-1), such that the waveform and measurements are displayed on the scope LCD display, whereas the X-Replay application and test results are displayed on a second monitor. When X-Replay is executed in the scope, the scope will appear as a local host (IP address is 127.0.0.1). To verify its correct operation, the following steps must be taken once the scope is turned on:

1. Minimize the X-Stream scope window.
2. Open X-Replay.
3. Select **Scope Manager**. The Scope Selector window will display the ID of the scope attached:

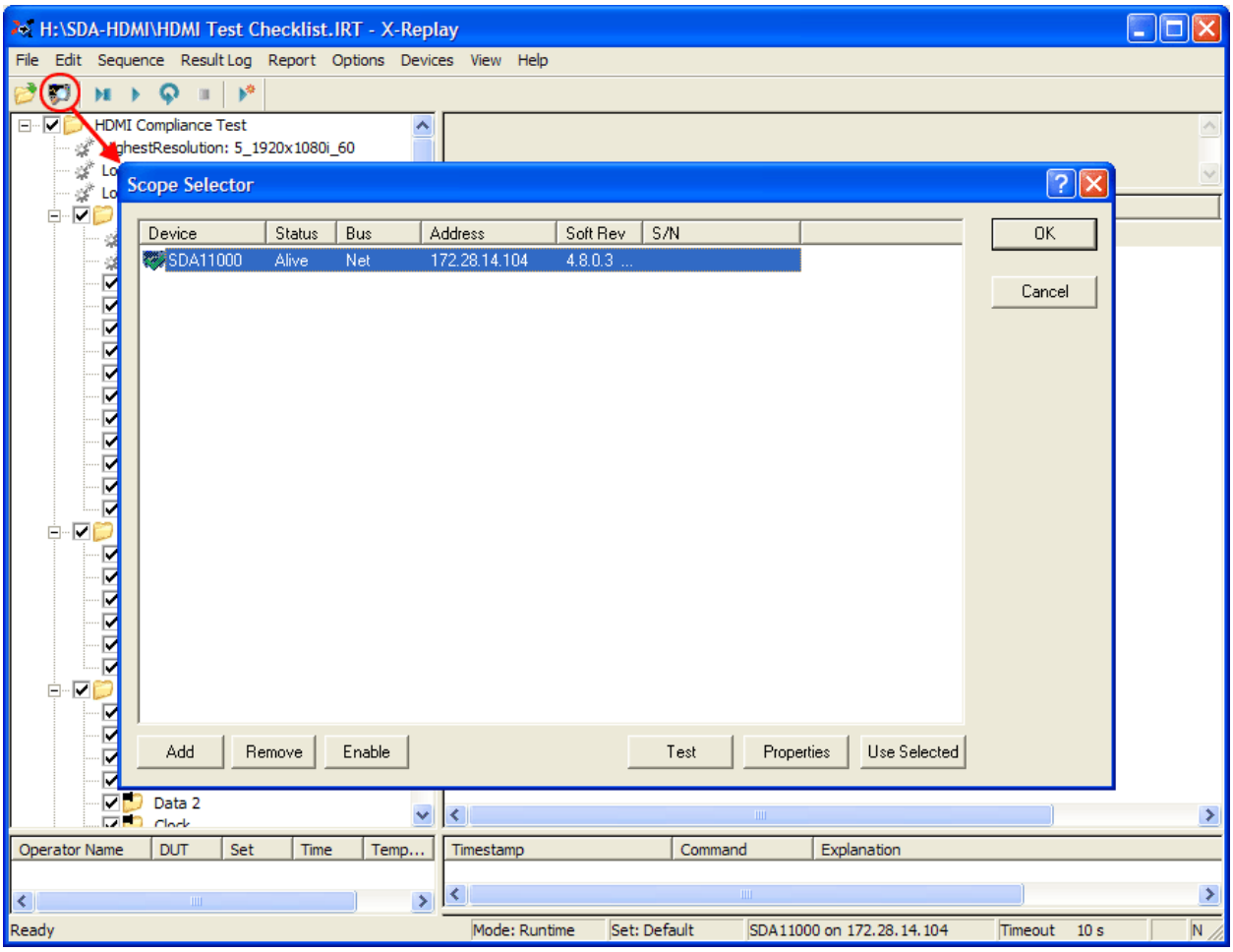


Figure 7. Selecting a scope

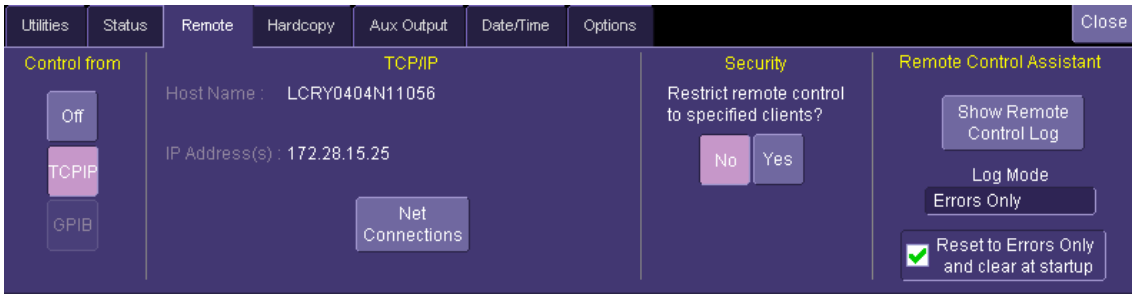
4. Press the **Test** button. If the scope is detected, a message box will indicate that the test is OK. X-Replay is now ready for use.

Remote (Networked) Configuration

Of course, it is also possible to run SDA-HDMI by installing X-Replay in a host PC and controlling the scope through a Windows Network/LAN connection, which allows you to control other instruments or run applications from the host PC (for example, setting up and configuring the LeCroy PE Protocol and Host Emulator instruments). The scope must already be configured, and an IP address (fixed or network-assigned) must already be established.

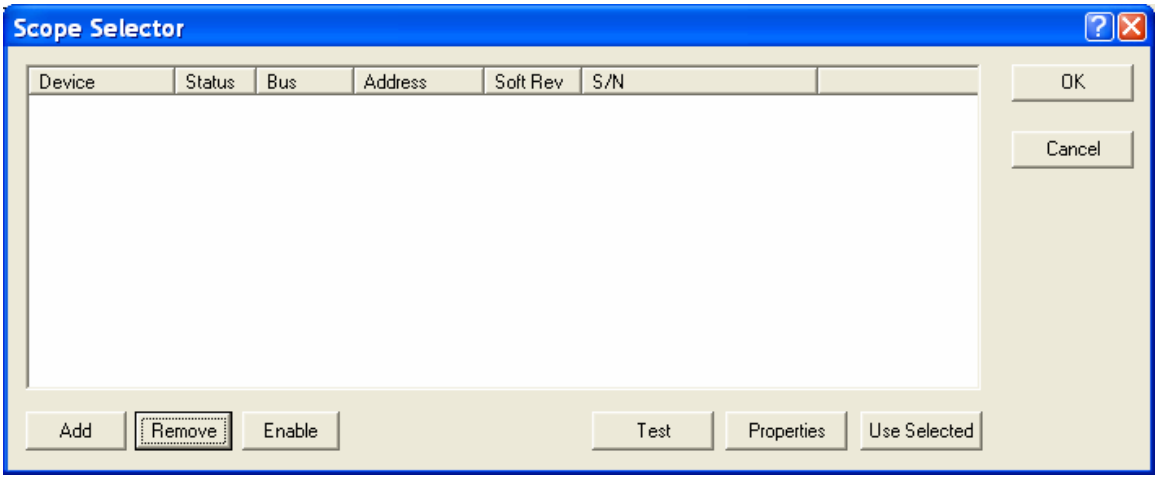
As an example of how to set up the scope using X-Replay over a LAN, follow these steps:

1. Verify in the **Utilities**, **Remote** dialog that the scope has an assigned IP address, and control is set to TCP/IP as shown below.

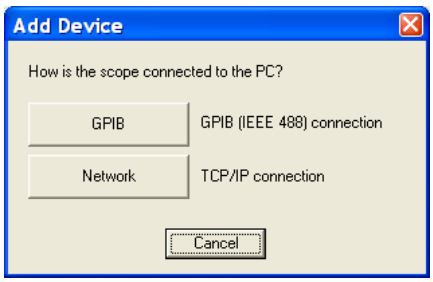


2. Make sure that the host PC is connected to the same LAN as the scope. If unsure, contact your system administrator.

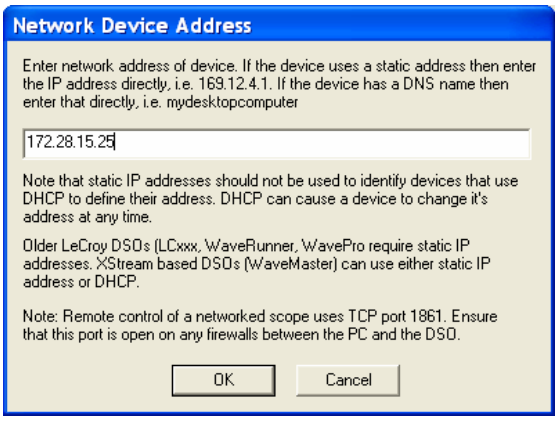
3. Open **X-Replay** in the host PC and select **Devices**, **Scope Manager**; the Scope Selector window opens. There should be no devices enabled at this time:



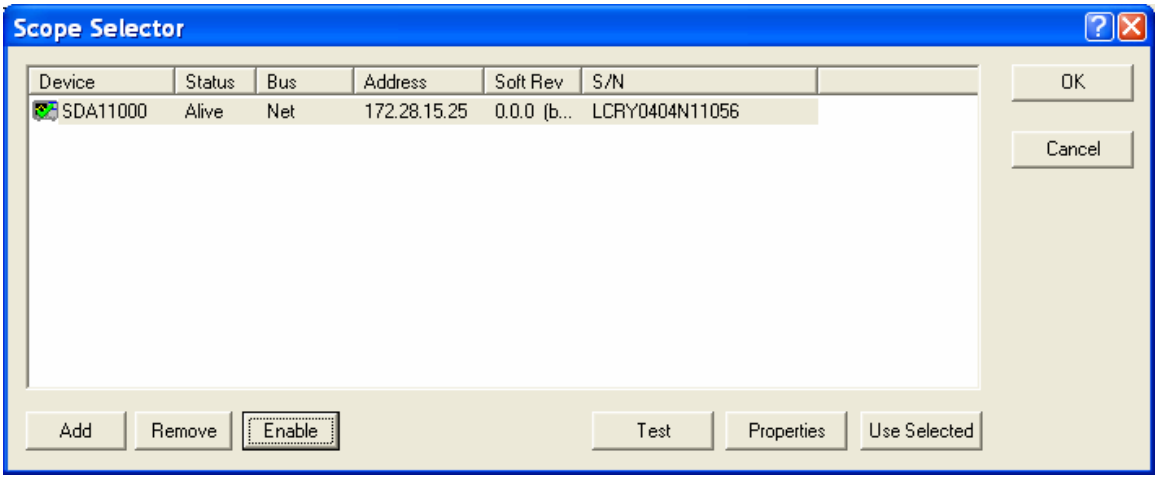
4. Click the **Add** button. Select the connection method (**GPIB** or **Network**):



5. In this example, we select **Network**, then enter the **IP address** from step #1:



6. Click **OK**. The Scope Selector window will display the correct information about the scope connected to the LAN. In this example, an SDA 11000 is connected as shown below:



7. Run X-Replay. The program will take control of the scope.

CHECKLIST TEST MODE OF OPERATION

This section covers use of X-Replay and the supplied “HDMI Compliance Test.irt” script to perform tests described in the PHY Electrical Test Considerations, and generating a report from X-Replay using the supplied style sheet “XReplayHDMI_Report.xslt”

X-Replay allows you to test HDMI functionality in several ways:

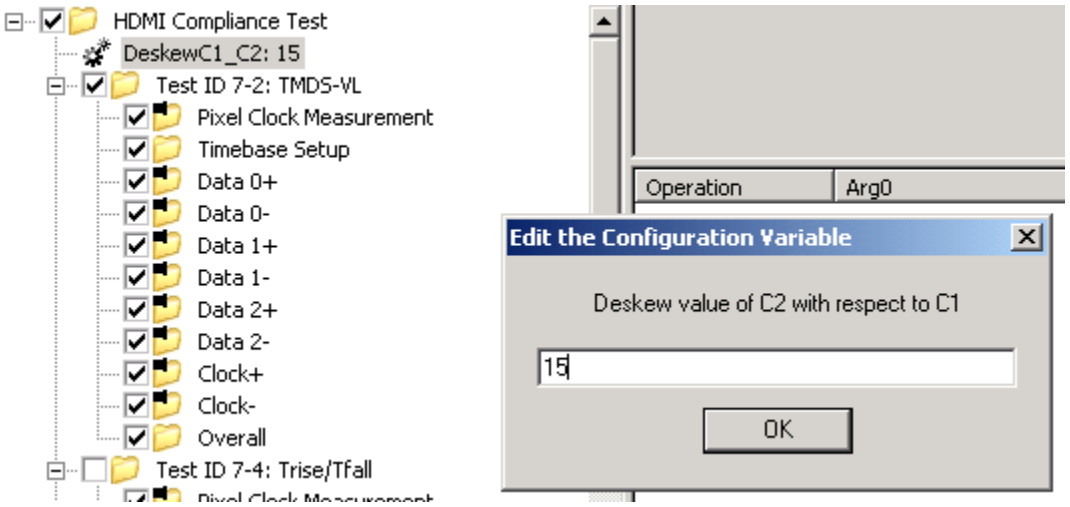
- Select, repeat, and skip tests as required to demonstrate or develop different PHY functions.
- Establish Test Limits for each of the versions of the HDMI specification and modify, import, or delete entire test limit sets.
- Generate Test Reports based on the tests actually run.
- Query the database for test results from prior test sessions or experimental runs.

The X-Replay application window is divided into several panes (clockwise, from upper left hand):

- Test Sequence pane
- Test Description pane
- Commands pane
- Activity Log pane
- Session pane

Use of Configuration Variables in Test Sequences

Configuration Variables allow you to define system inputs such as signal sources, probe types, specification parameter set to be used for testing, form factors, and other global conditions. These variables can be set prior to beginning tests, or changed between test runs.



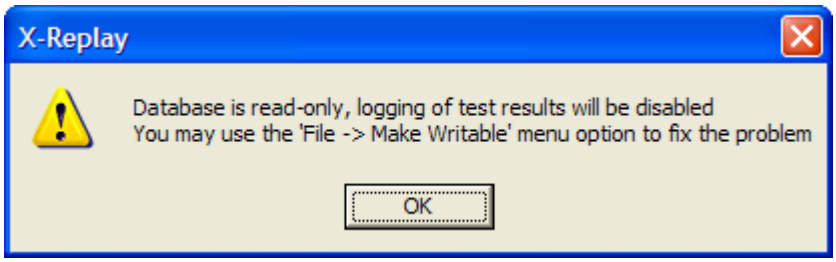
Right-clicking on any variable and selecting **Change value** allows you to reset the variable to its default setting, or to change the value to be used for subsequent tests.

Menu Structure

File

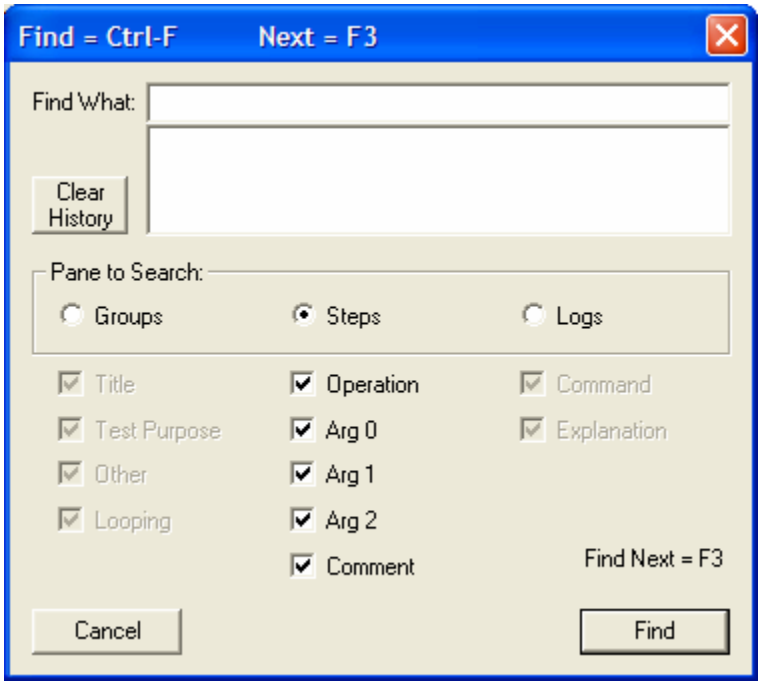
Open Test Database. The file extension is *.irt

Make Read Only disables writing of test results into session log. *Make Writable* reverses the action.



Edit

Performs the find function to locate specific measurements or actions in the program sequence.



Sequence

Execute program items starting at the designated point. The toolbar displays the available choices, from left to right:

Open

Search Attached Devices performs a scope search.

Single Step [F10] executes one instruction at a time.

Play Selected Group and Children [F5] executes all the checked items in the selected group.

Play Selected Group Continuously executes all checked items in the selected group until *Stop* is selected.

Stop stops execution (active when *Play* has been pressed).

Start a New Test Session

Result Log

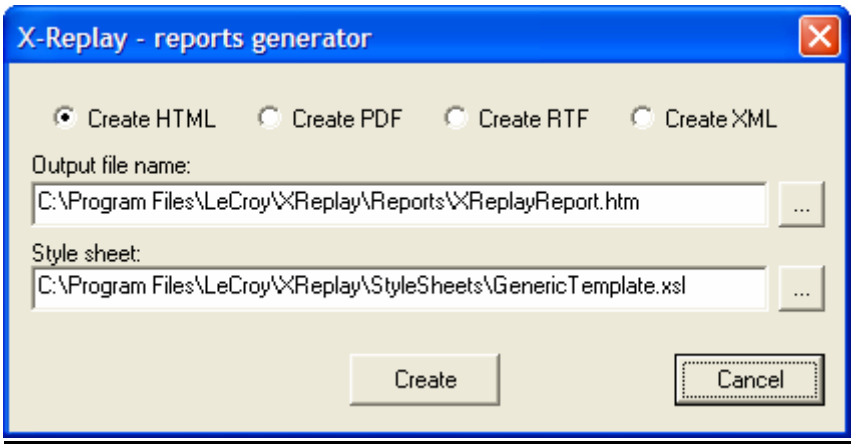
Clear Log removes all the previously recorded activity.

Export to File (ASCII) creates a comma-separated-values set of activity records.

Export to File (ASCII) Standard creates a text file phy tests checklist.logdump.txt

Report

Creates a report in one of three formats (html, pdf, or rtf) based on the specified report template Style Sheet (*.xsl or *.xslt). For Style Sheet, please select the supplied “XReplayReport.xsl”. The “…” button to the right of the text entry field can be used to locate the file. On an SDA, it can be found in D:\Applications\HDMI.



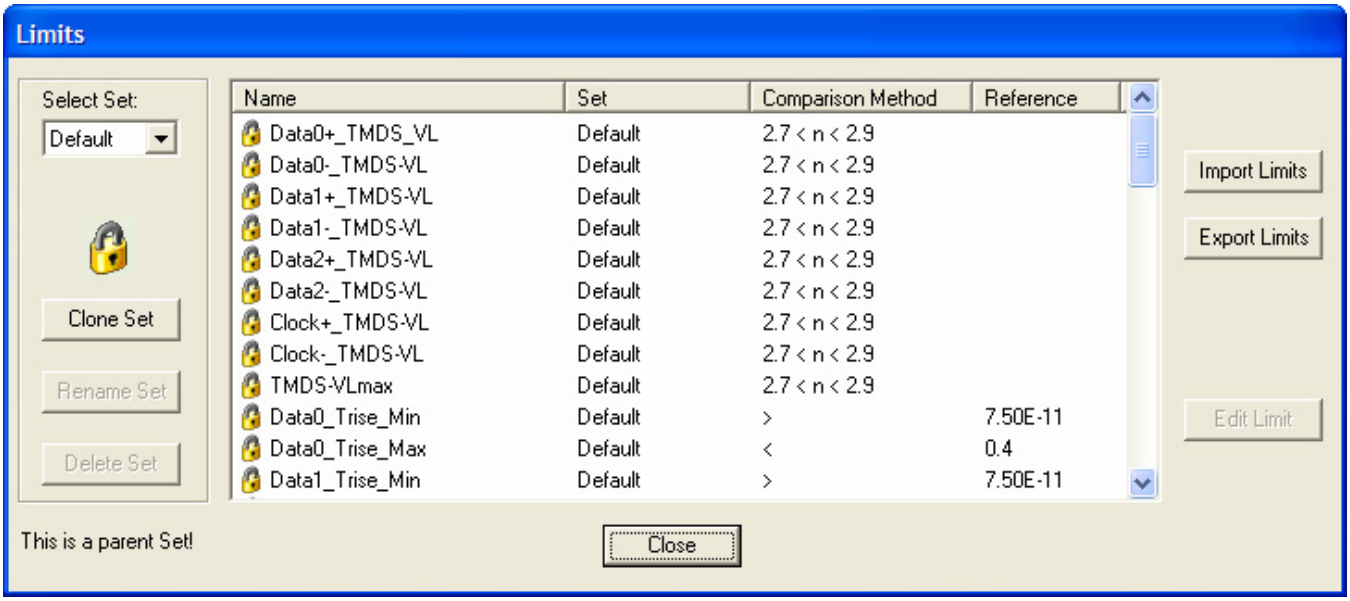
Options

Select the **Limits** option to allow the configuration of individual parameters pass/fail criteria, or to edit, rename, and save complete parameter sets.

Clone Set : You can create a new, named set of limits . Initially, the new set is the same as the set selected when selecting “Create Set”.

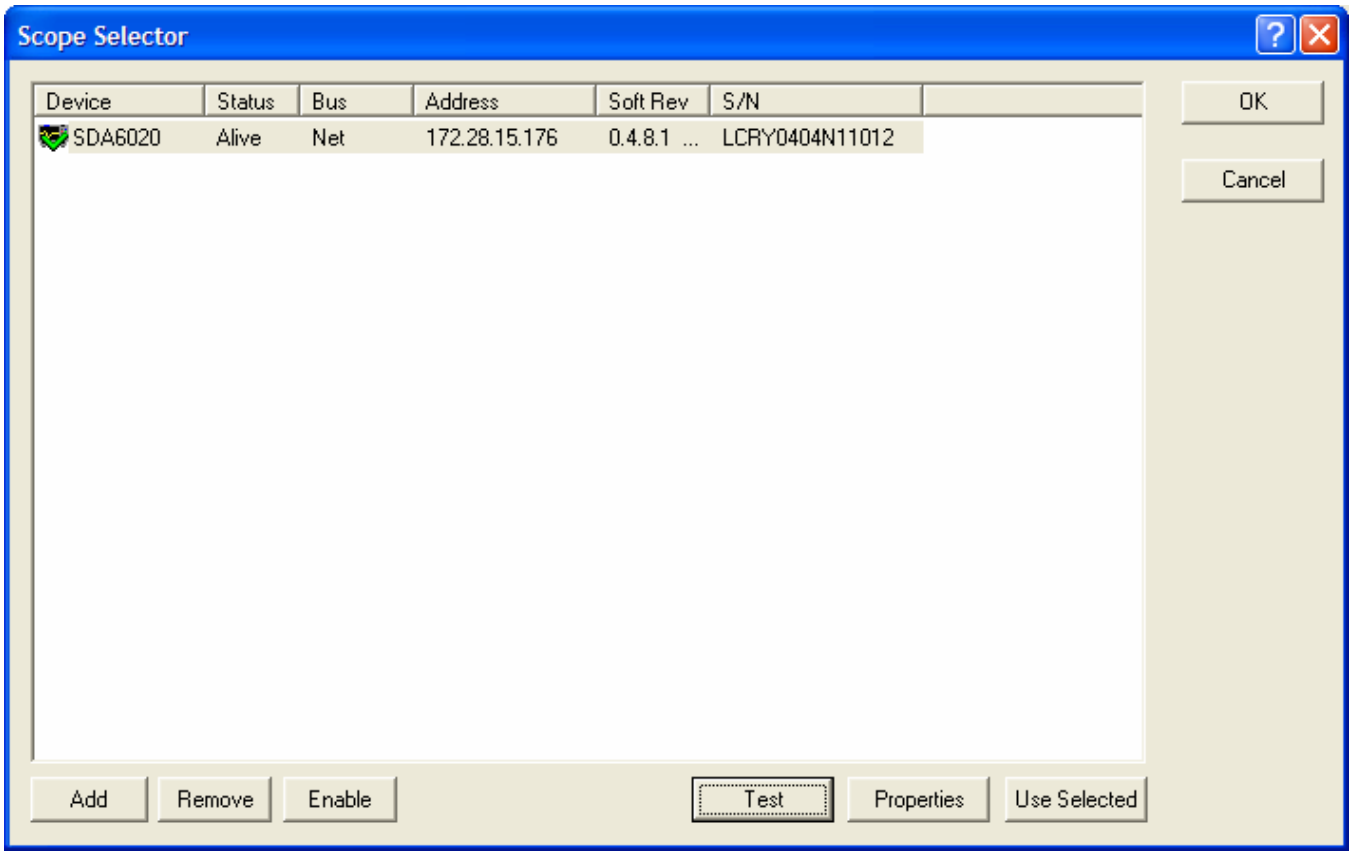
Edit Limit: Using Edit Limit allows limits to be changed to meet specific pass/fail criteria.

Import/Export Limits allows you to transfer entire parameter sets to csv-formatted (MS Excel) files

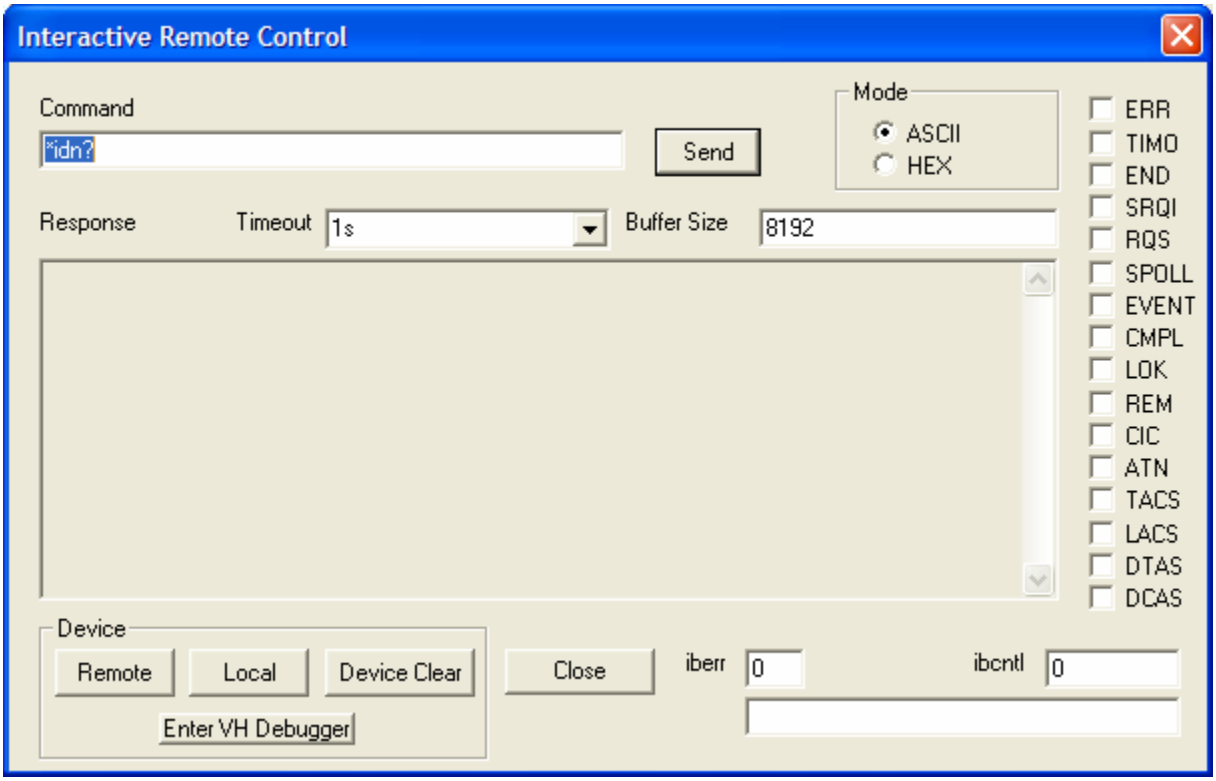


Devices

Scope Manager displays the devices connected to the host computer. There are two supported modes of attaching a device: GPIB or LAN.



Interactive Dialog supports sending and receiving of single line commands to the devices in the list.



View

Shows/hides toolbar and status bars.

Help

Help Topics

Running HDMI Tests

1. Verify proper signal input and perform all deskew and calibration procedures.
2. Run X-Replay application.
3. Select **File**, **Open Test Database**, and open the HDMI PHY Tests database.
4. Select the test groups to be executed. By default, all test groups and individual tests within each group are selected. However, you can uncheck any tests you do not want to run.
5. Set up configuration variables as required for the selected tests by right-clicking the variable and selecting **Change value**.
6. Select **Start a new test session**  and follow script prompts, as required.

*Export to *.XML file – Database Access*

X-Replay allows you to export entire test sessions in XML file format for subsequent access by database programs such as Microsoft Access. Most database programs have built-in XML import data capability. Please note that test sessions appear at the lower left portion of the X-Replay screen.

In order to create an XML record of the session data, right-click on the desired test session and select **Dump Log into XML**.

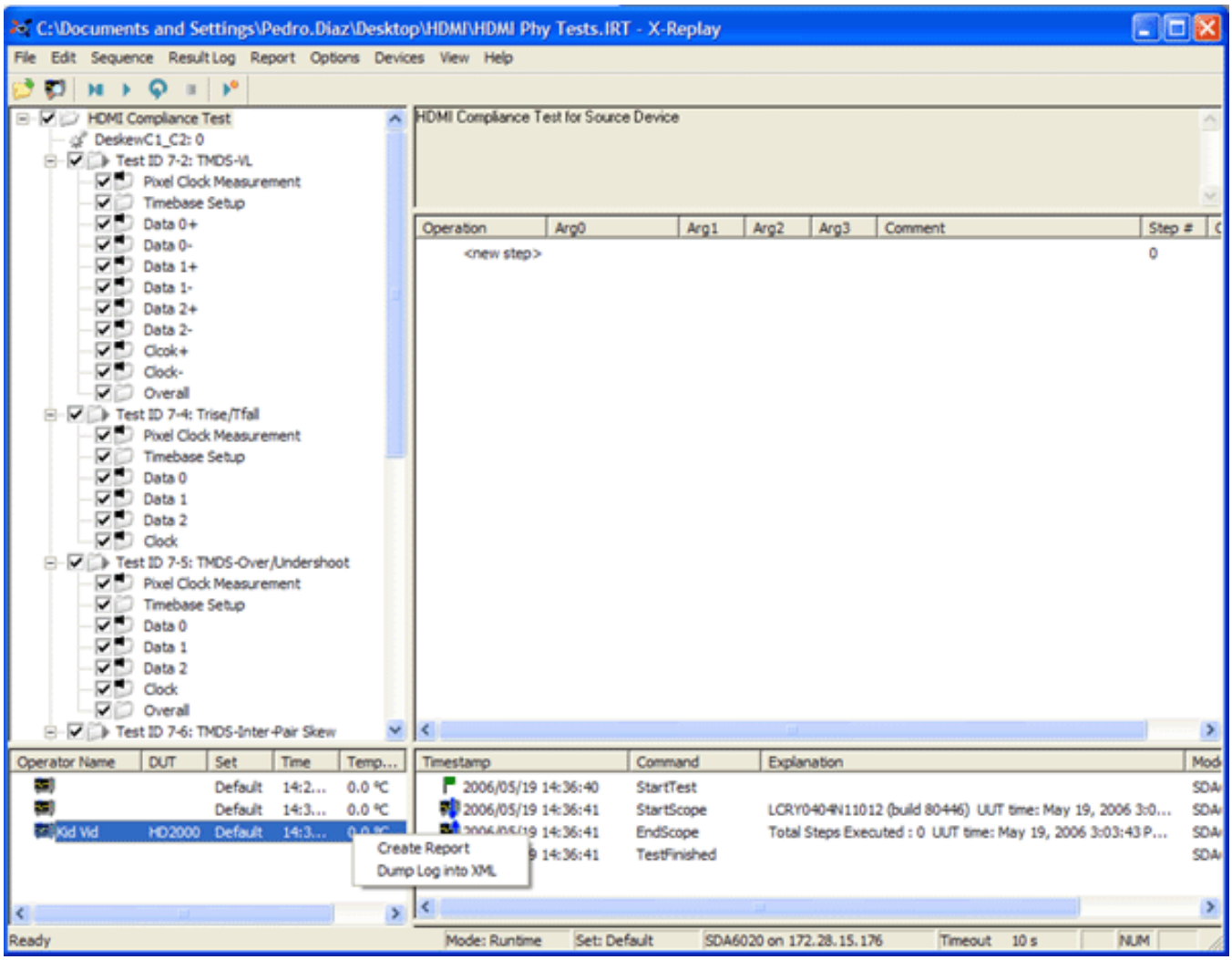


Figure 8. Saving test results in xml format

TEST SEQUENCE REFERENCE

General Information (Batch/Device Info)

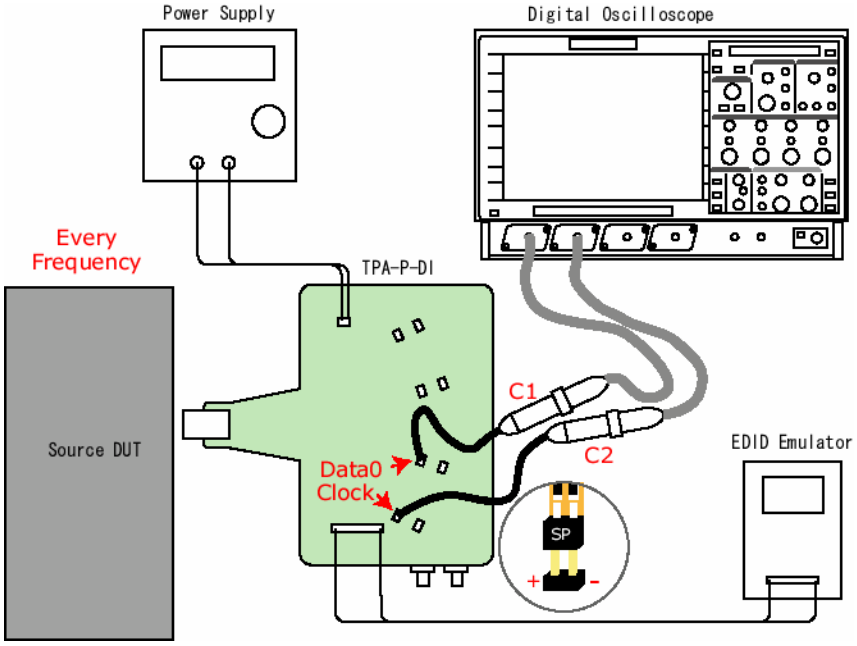
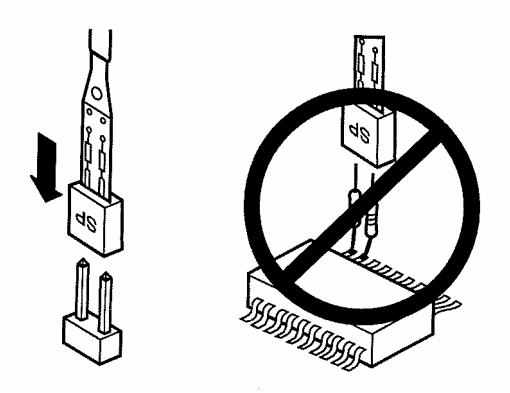


Figure 9. Note in the Figure above that "P" on the connector aligns with the negative pin. That is, "P" does not mean "positive." When connecting the probe to the scope, use an LPA-BNC adapter; do not plug the probe directly into the scope panel without an adapter.



Some tests require multiple changes of test fixtures.

Device Info

Purpose: Space provided to enter device-specific information (alphanumeric)

Available Entries:

Enter first Lane ID

Enter second Lane ID

HDMI Tests

Source Device Tests

Test ID 7-2: TMDS-V_L

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the DC specification in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals."

[HDMI: Table 4-12] Source DC Characteristics at TP1

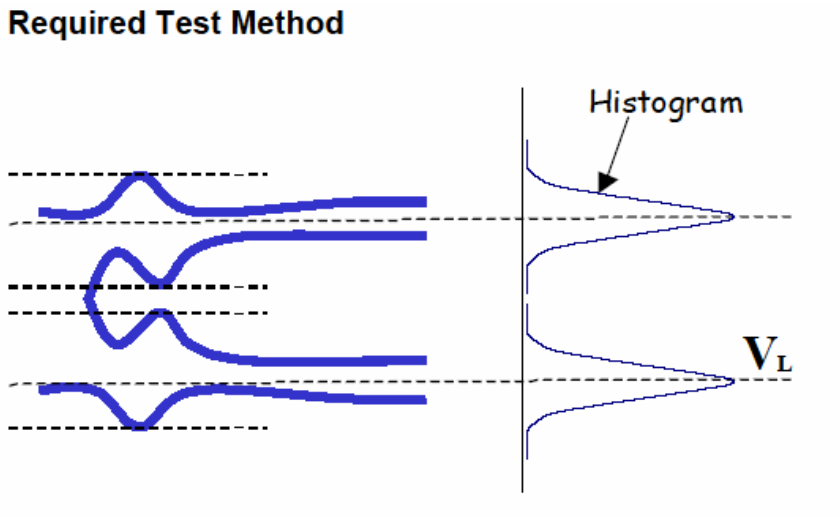
Single-ended low level output voltage, V_L

(Avcc-600mV) <= V_L <= (Avcc-400mV)

Test Objective:

Confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

Required Test Method



Test Conditions:

Test Fixture	TF-HDMI TPA-P-SE
Probe	D350-ST/SP on Channel 1
Display Resolution	Lowest supported pixel clock frequency

Test procedure:

1. Connect TPA-P-SE adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with lowest supported pixel clock frequency.
3. Connect probe to TMDS_DATA0+.
4. Capture waveform more than $2T_{BIT}$ duration 10,000 times as segments in sequence trigger mode.
5. Calculate V_L using histogram method

   If (V_L > 2.900 V) OR (V_L < 2.700 V) then FAIL
6. Repeat same procedure on all HDMI signal links.

Test ID 7-4: TMDS-T_{RISE},T_{FALL}

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

[HDMI: Table 4-13] Source AC Characteristics at TP1

75 ps <= Rise Time or Fall Time <= 0.4 * T_{BIT}

Test Objective:

Confirm that the rise time and fall time on the TMDS differential signals fall within the limit of the specification.

Test Conditions:

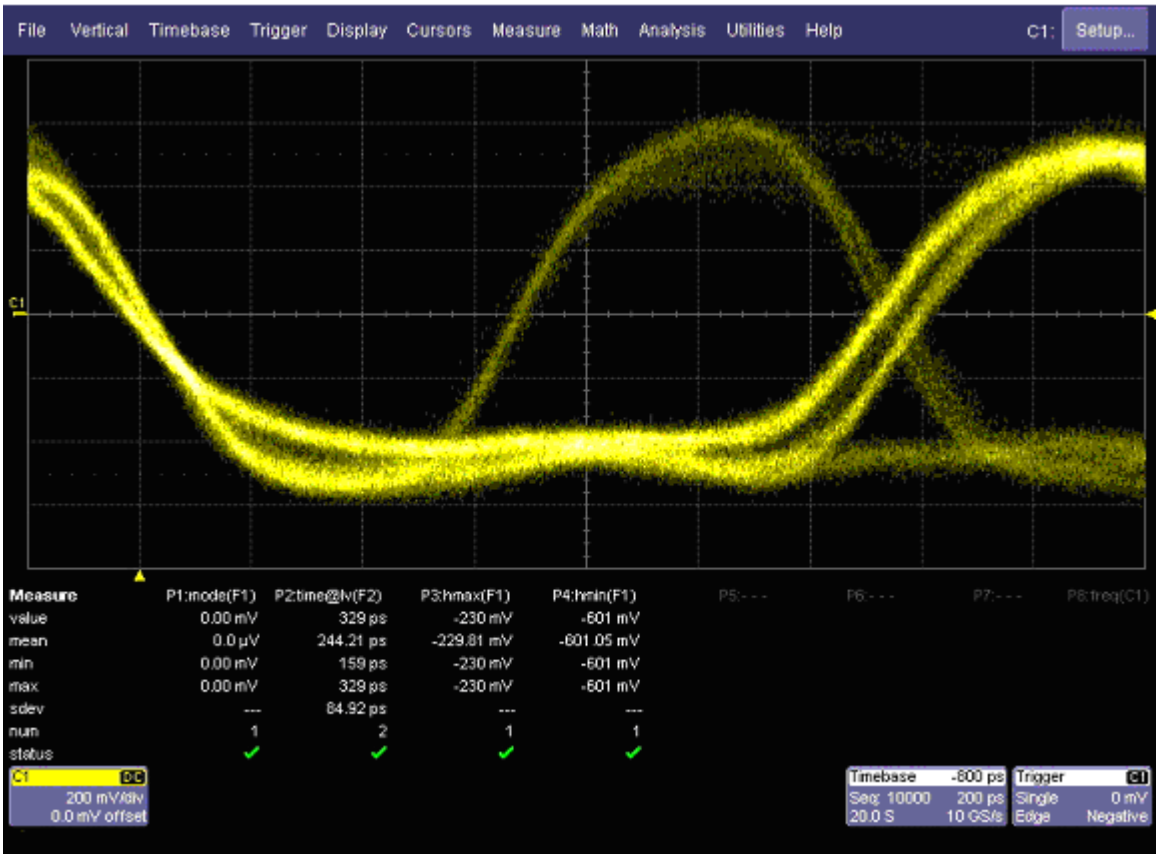
Test Fixture	TF-HDMI TPA-P-DI
Probe	D350-ST/SP on Channel 1
Display Resolution	Highest supported pixel clock frequency

Test procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with highest supported pixel clock frequency
3. Connect probe to TMDS_DATA0.
4. Capture waveform more than 2TBIT duration 10,000 times as segments in sequence trigger mode.

   If (T_{RISE} < 75 ps) OR (T_{RISE} > 0.4 * T_{BIT}) then FAIL

   If (T_{FALL} < 75 ps) OR (T_{FALL} > 0.4 * T_{BIT}) then FAIL
5. Repeat same procedure on all HDMI differential signal links.



Test ID 7-5: TMDS Over/Undershoot

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

[HDMI: Table 4-13] Source AC Characteristics at TP1

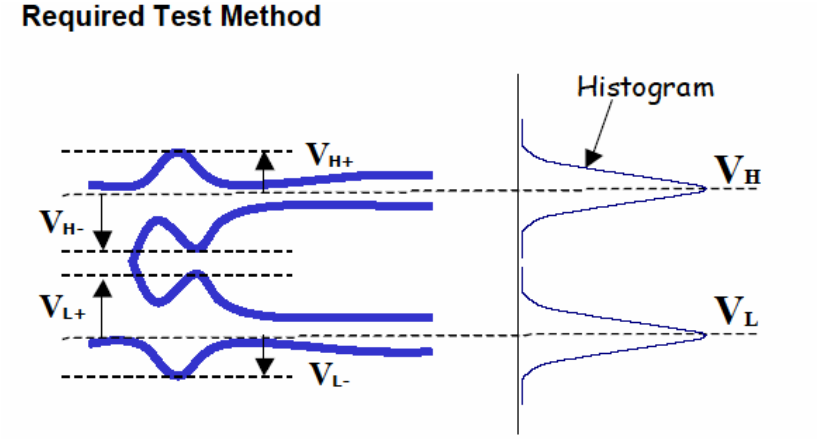
TMDS overshoot must be <= 15% of 2 * V_{SWING}

TMDS undershoot must be <= 25% of 2 * V_{SWING}

Test Objective:

Confirm that the differential TMDS signals do not have overshoot and undershoot beyond that allowed by the specification.

Required Test Method



Test Conditions:

Test Fixture	TF-HDMI TPA-P-DI
Probe	D350-ST/SP on Channel 1
Display Resolution	Lowest supported pixel clock frequency

Test Procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with lowest supported pixel clock frequency.
3. Connect probe to TMDS_DATA0.
4. Capture waveform more than 2TBIT duration 10,000 times as segments in sequence trigger mode.

   If Overshoot > 15% of 2*VSWING then FAIL

   If Undershoot > 25% of 2*VSWING then FAIL
5. Repeat same procedure on all HDMI differential signal links.

Test ID 7-6: TMDS Inter-Pair Skew

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

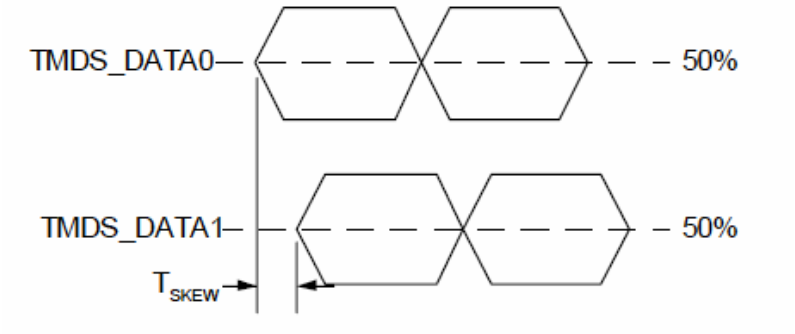
[HDMI: Table 4-13] Source AC Characteristics at TP1

Inter-Pair skew must be exceed 0.20 * T_{PIXEL}.

Test Objective:

Confirm that any skew between the differential pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Required Test Method



Test Conditions:

Test Fixture	TF-HDMI TPA-P-DI
Probe	Two of D350-ST/SPs on Channel 1 and Channel 2
Display Resolution	Highest supported pixel clock frequency

Test Procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with highest supported pixel clock frequency.
3. Connect probe to TMDS_DATA0 and TMDS_DATA1.
4. Capture waveform more 1M waveform as singleshot

   If (skew > 0.15*TBIT) then FAIL
5. Repeat same procedure on all combination of HDMI differential signal links.

Test ID 7-7: TMDS Intra-Pair Skew

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

[HDMI: Table 4-13] Source AC Characteristics at TP1

Intra-Pair skew must be exceed 0.15 * T_{PIXEL}.

Test Objective:

Confirm that any skew within any one differential pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Test Conditions:

Test Fixture	TF-HDMI TPA-P-SE
Probe	Two of D350-ST/SPs on Channel 1 and Channel 2
Display Resolution	Highest supported pixel clock frequency

Test procedure:

1. Connect TPA-P-SE adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with highest supported pixel clock frequency.
3. Connect probe to TMDS_DATA0+ and TMDS_DATA0-.
4. Capture waveform more 1M waveform as single shot.

   If (skew > 0.15*TBIT) then FAIL
5. Repeat same procedure on all HDMI differential signal links.

Test ID 7-8: TMDS Clock Duty Cycle

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

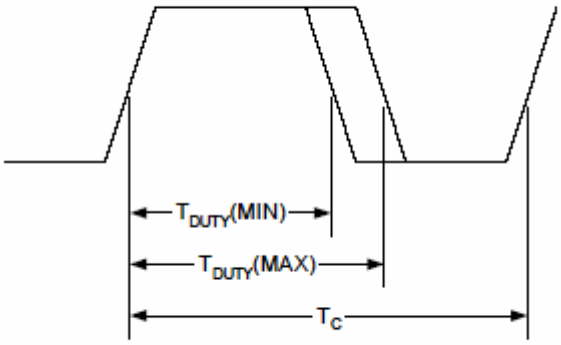
[HDMI: Table 4-13] Source AC Characteristics at TP1

Clock duty cycle must be at least 40% and not more than 60%.

Test Objective:

Confirm that the duty cycle of the differential TMDS clock does not exceed the limits in the specification.

Required Test Method



TMDS AC Clock Duty

Test Conditions:

Test Fixture	TF-HDMI TPA-P-DI
Probe	Two of D350-ST/SP on Channel 1
Display Resolution	Highest supported pixel clock frequency

Test procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with highest supported pixel clock frequency.
3. Connect probe to TMDS_Clock.
4. Capture waveform 2M points as single shot.

   If (T_{DUTY}(MIN) < 40%) OR (T_{DUTY}(MAX) > 60%) then FAIL

Test ID 7-9: TMDS Clock Jitter

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"The Source shall meet the AC specification in Table 4-13 across all operating conditions specified in Table 4-11."

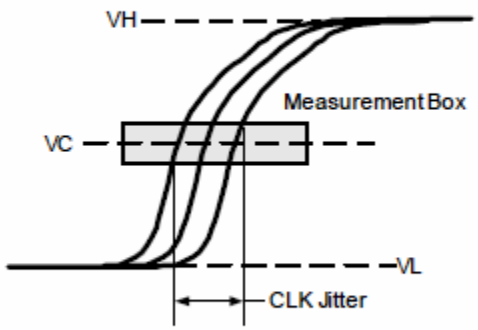
[HDMI: Table 4-13] Source AC Characteristics at TP1

TMDS differential clock jitter must not exceed 0.25 * T_{BIT}, relative to the ideal Recovery Clock.

Test Objective:

Confirm that the TMDS Clock does not carry excessive jitter.

Required Test Method



TMDS AC Clock Jitter

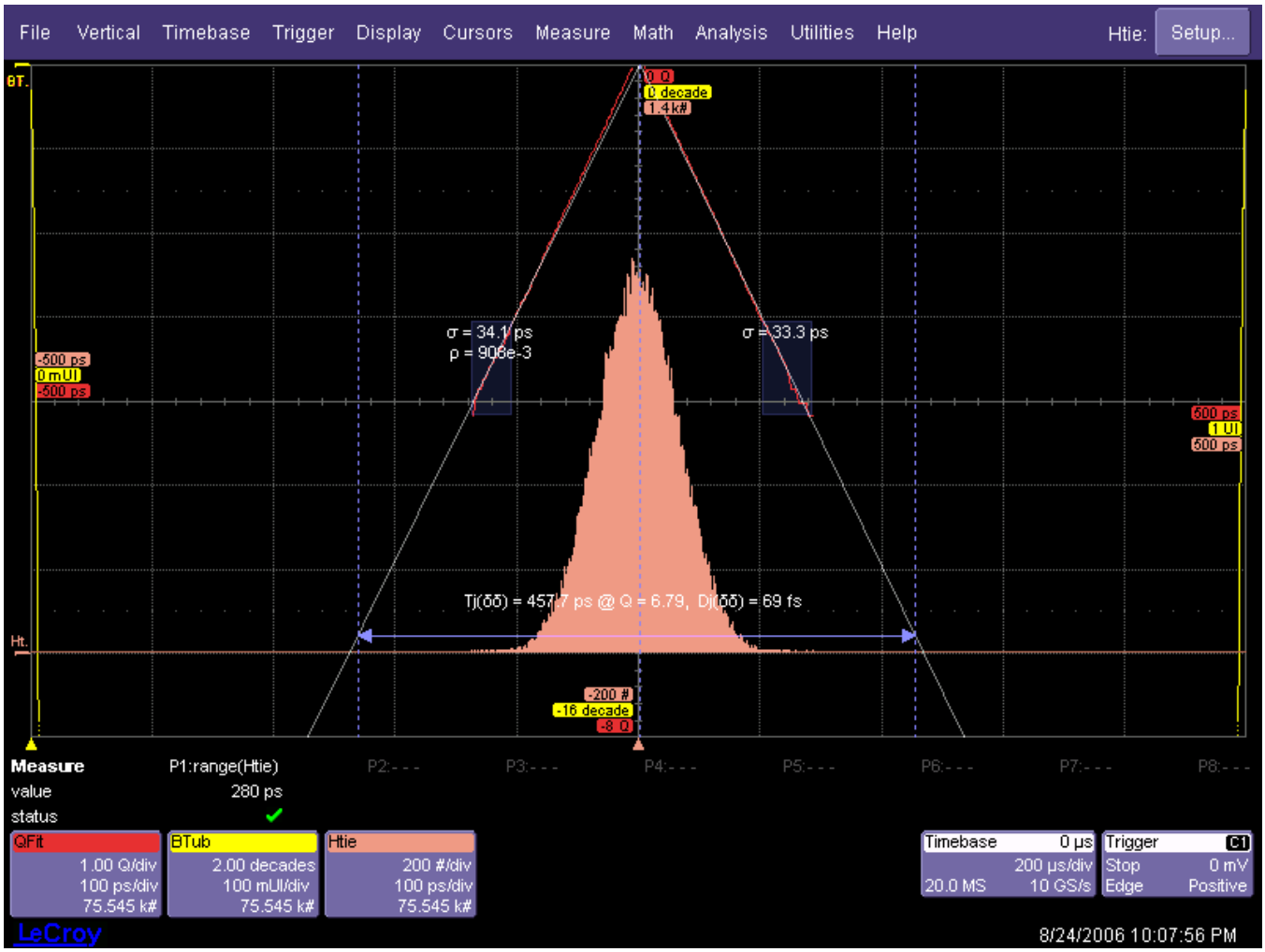
Test Conditions:

Test Fixture	TF-HDMI TPA-P-DI
Probe	Two of D350-ST/SP on Channel 1
Display Resolution	Highest supported pixel clock frequency

Test procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with highest supported pixel clock frequency.
3. Connect probe to TMDS_Clock.
4. Capture waveform 16M points as single shot.

   If Clock jitter exceeds 0.25* TBIT -> then FAIL.



Test ID 7-10: TMDS Data Eye Diagram

Reference:

[HDMI: 4.2.4] HDMI Source TMDS Characteristics

"For all channel under all operating conditions specified in Table 4-11…the Source shall have output level at TP1, which meet the normalized eye diagram requirements of Figure 4-12."

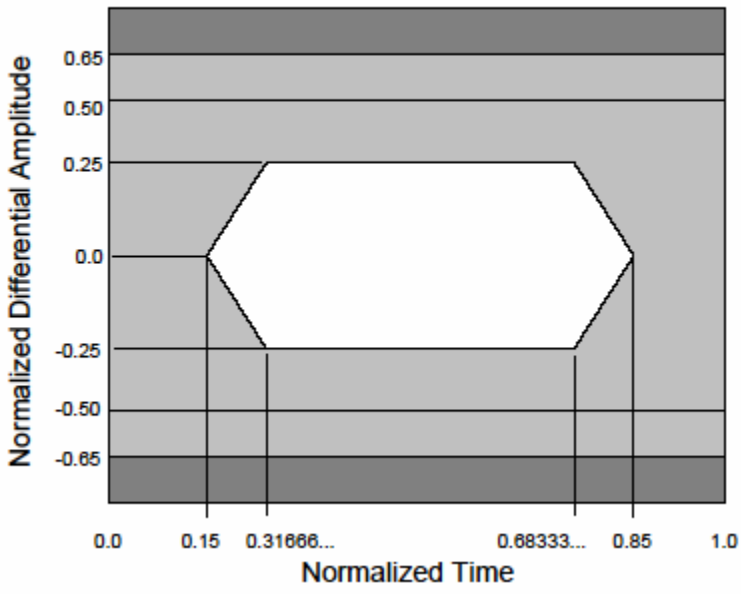
[HDMI: Figure 4-12] Normalized Eye Diagram Mask at TP1

Refer to the [HDMI: Figure 4-12] "Normalized Eye Diagram Mask at TP1 for Source Requirements".

Test Objective:

Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits of eye opening in the specification.

Required Test Method

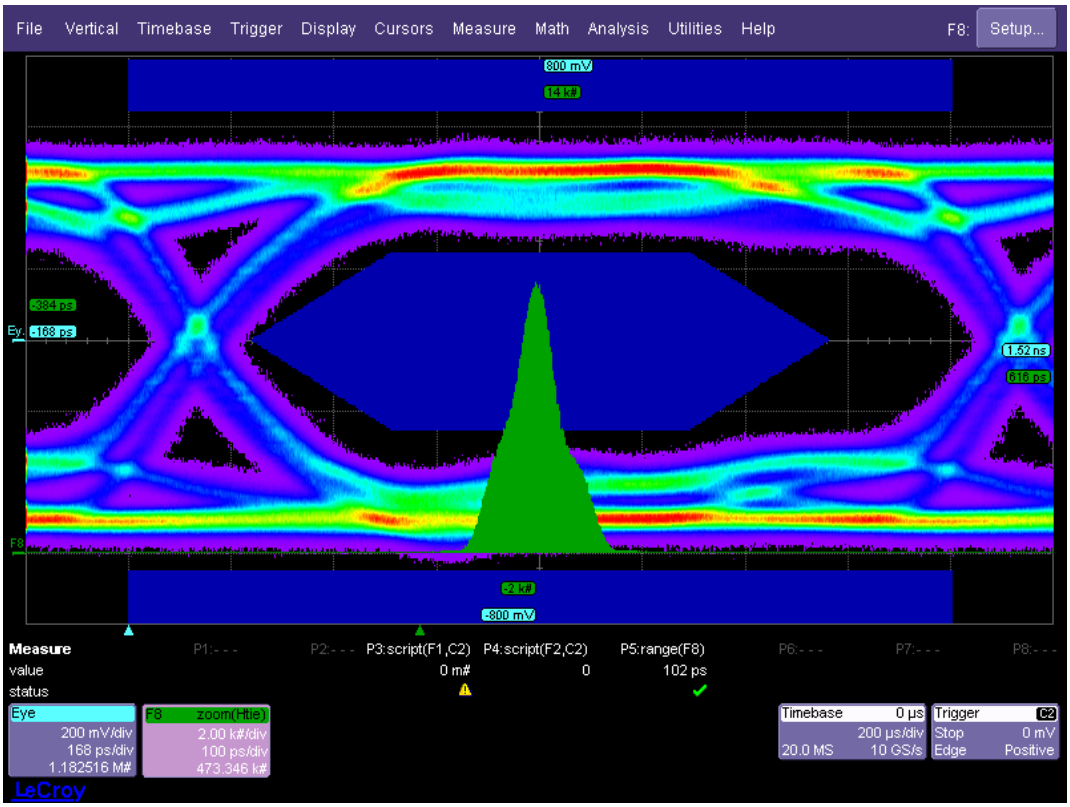


Test Conditions:

Test Fixture	TF-HDMI TPA-P-DI
Probe	Two of D350-ST/SPs on Channel 1 and Channel 2
Display Resolution	All supported pixel clock frequency

Test Procedure:

1. Connect TPA-P-DI adapter to Source DUT HDMI output connector.
2. Set the Source DUT to output a video format with Lowest supported pixel clock frequency.
3. Connect probe from C1 to TMDS_DATA0 and from C2 to TMDS_Clock.
4. Capture waveform 16M points as single shot.
5. Compare the data eye to the TP1 Eye Diagram Mask.
6. Shift the mask left until one of the left-side corners touches the waveform.
   If any other part of the waveform touches or crosses into the data eye then FAIL
   If data jitter > 0.3*TBIT then FAIL
7. Repeat all HDMI differential signal links with all supported pixel clock frequency.


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
F8: Setup...
800 mV
14 k#
-384 ps
Eye -168 ps
1.52 ns
0.16 ps
F8
-2 k#
-800 mV
Measure
P1:- - -
P2:- - -
P3:script(F1,C2)
P4:script(F2,C2)
P5:range(F8)
P6:- - -
P7:- - -
P8:- - -
value
0 m#
0
102 ps
status
Eye
200 mV/div
168 ps/div
1.182516 M#
F8 zoom(Htie)
2.00 k#/div
100 ps/div
473.346 k#
Timebase 0 µs
200 µs/div
20.0 MS 10 GS/s
Trigger C2
Stop 0 mV
Edge Positive
LeCroy

§ § §

HDMI Test Results Source DUT

Overall result: Fail

DUT: New_RevA
Limits in use: Default
Scope SN: LCRY0401N00813
Scope Name: LCRY0401N00813
Operator: James
Computer: LCRY0401N00813
Time of test: 08/24/2006 21:39:08
Temperature: 32.000000? C

Summary Table

ID	Pass/Fail	Comment
7-2 **TMDS-VL**	Fail	VL_Max4 = 2.664V D0+ = 2.664V , D0- = 2.646V D1+ = 2.646V , D1- = 2.651V D2+ = 2.651V , D2- = 2.660V CK+ = 2.651V , CK- = 2.651V
7-4 **TMDS-Trise, Tfall**	Pass	_____Trise_____Tfall_____ D0: 253.652psec (NaNTbit) , 218.801psec (NaNTbit) D1: 230.879psec (NaNTbit) , 228.486psec (NaNTbit) D2: 235.436psec (NaNTbit) , 210.252psec (NaNTbit) CK: 236.481psec (NaNTbit) , 254.067psec (NaNTbit)
7-5 **TMDS-Over/Undershoot**	Pass	Overshoot = 10.526% Undershoot = 16.667%
7-6 **TMDS-Inter_Pair Skew**	Fail	TIPSKEW_MAX = 27,553,652.247Tpixel D0-D1: 27,553,652.247Tpixel D1-D2: 1.017E -03Tpixel D0-D2: 27,553,652.247Tpixel D1-CK: 3.826E -02Tpixel D0-CK: 1.017E -03Tpixel D2-CK: 4.632E -02Tpixel
7-7 **TMDS-Intra_Pair Skew**	Fail	TXPSKEW_MAX = 0.900Tbit D0: 0.253Tbit D1: 0.900Tbit D2: -5.136E -02Tbit CK: 0.933Tbit
7-8 **TMDS-Clock Duty Cycle**	Pass	Clock Duty: Min=49.905% Clock Duty: Max= 50.148%

7-9 **TMDS-Clock Jitter**	Pass	Clock Jitter =0.069Tbit
7-10 **TMDS-Data Eye Diagram**		

Details

7-2 TMDS-VL

Tbit for Low Level Output Voltage Test

Pass

Limit Name: Tbit
Current Value: 4.07405243456663E-09
Test Criteria: > 0
Timestamp: 2006/08/24 21:41:09

Low Level Output Voltage of Data 0+

Fail

Failure Explanation: Current value 2.66412 outside the Limit Data0+_TMDS_VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data0+_TMDS_VL
Current Value: 2.66412105784189
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:42:25

Low Level Output Voltage of Data 0-

Fail

Failure Explanation: Current value 2.64644 outside the Limit Data0-_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data0-_TMDS-VL
Current Value: 2.64644321878094
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:45:00

Low Level Output Voltage of Data 1+

Fail

Failure Explanation: Current value 2.64644 outside the Limit Data1+_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data1+_TMDS-VL
Current Value: 2.64644321878094
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:45:45

Low Level Output Voltage of Data 1-

Fail

Failure Explanation: Current value 2.65086 outside the Limit Data1-_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data1-_TMDS-VL
Current Value: 2.65086267854617
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:45:56

Low Level Output Voltage of Data 2+

Fail

Failure Explanation: Current value 2.65086 outside the Limit Data2+_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data2+_TMDS-VL
Current Value: 2.65086267854617
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:46:13

Low Level Output Voltage of Data 2-

Fail

Failure Explanation: Current value 2.6597 outside the Limit Data2-_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Data2-_TMDS-VL
Current Value: 2.65970159807665
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:46:50

Low Level Output Voltage of Clock+

Fail

Failure Explanation: Current value 2.65086 outside the Limit Clock+_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Clock+_TMDS-VL
Current Value: 2.65086267854617
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:47:24

Low Level Output Voltage of Clock-

Fail

Failure Explanation: Current value 2.65086 outside the Limit Clock-_TMDS-VL Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: Clock-_TMDS-VL

Current Value: 2.65086267854617
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:47:36

Maximum Low Level Output Voltage

Fail

Failure Explanation: Current value 2.66412 outside the Limit TMDS-VLmax Lower limit: 2.7, Upper limit: 2.9 Within limit test failed
Limit Name: TMDS-VLmax
Current Value: 2.66412105784189
Test Criteria: 2.7 < n < 2.9
Timestamp: 2006/08/24 21:47:36

7-4 Trise/Tfall

Tbit for Trise/Tfall Test

Pass

Limit Name: Tbit
Current Value: 4.07410622373607E-09
Test Criteria: > 0
Timestamp: 2006/08/24 21:48:54

Minimum Rise Time of Data 0

Pass

Limit Name: Data0_Trise_Min
Current Value: 253.651962280273
Test Criteria: > 75
Timestamp: 2006/08/24 21:49:50

Maximum Rise Time of Data 0

Pass

Limit Name: Data0_Trise_Max
Current Value: 6.22595357976865E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:49:50

Minimum Fall Time of Data 0

Pass

Limit Name: Data0_Tfall_Min
Current Value: 218.801116943359
Test Criteria: > 75

Timestamp: 2006/08/24 21:49:55

Maximum Fall Time of Data 0

Pass

Limit Name: Data0_Tfall_Max
Current Value: 5.37053049006446E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:49:55

Minimum Rise Time of Data 1

Pass

Limit Name: Data1_Trise_Min
Current Value: 230.879440307617
Test Criteria: > 75
Timestamp: 2006/08/24 21:50:18

Maximum Rise Time of Data 1

Pass

Limit Name: Data1_Trise_Max
Current Value: 5.66699608769391E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:50:19

Minimum Fall Time of Data 1

Pass

Limit Name: Data1_Tfall_Min
Current Value: 228.486480712891
Test Criteria: > 75
Timestamp: 2006/08/24 21:50:24

Maximum Fall Time of Data 1

Pass

Limit Name: Data1_Tfall_Max
Current Value: 5.60826027023326E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:50:24

Minimum Rise Time of Data 2

Pass

Limit Name: Data2_Trise_Min

Current Value: 235.435562133789
Test Criteria: > 75
Timestamp: 2006/08/24 21:50:37

Maximum Rise Time of Data 2

Pass

Limit Name: Data2_Trise_Max
Current Value: 5.77882728639038E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:50:37

Minimum Fall Time of Data 2

Pass

Limit Name: Data2_Tfall_Min
Current Value: 210.251998901367
Test Criteria: > 75
Timestamp: 2006/08/24 21:50:42

Maximum Fall Time of Data 2

Pass

Limit Name: Data2_Tfall_Max
Current Value: 5.16069015766997E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:50:42

Minimum Rise Time of Clock

Pass

Limit Name: Clock_Trise_Min
Current Value: 236.481475830078
Test Criteria: > 75
Timestamp: 2006/08/24 21:51:04

Maximum Rise Time of Clock

Pass

Limit Name: Clock_Trise_Max
Current Value: 5.80449951089439E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:51:04

Minimum Fall Time of Clock

Pass

Limit Name: Clock_Tfall_Min
Current Value: 254.067153930664
Test Criteria: > 75
Timestamp: 2006/08/24 21:51:09

Maximum Fall Time of Clock

Pass

Limit Name: Clock_Tfall_Max
Current Value: 6.23614456713103E-02
Test Criteria: < 0.4
Timestamp: 2006/08/24 21:51:09

7-5 Over/Undershoot

Tbit for Over/Undershoot Test

Pass

Limit Name: Tbit
Current Value: 4.07407546104063E-09
Test Criteria: > 0
Timestamp: 2006/08/24 21:51:24

Overshoot of Data 0

Pass

Limit Name: Data0_Overshoot
Current Value: 0.105263157894737
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:51:40

Undershoot of Data 0

Pass

Limit Name: Data0_Undershoot
Current Value: 0.126315789473684
Test Criteria: < 0.25
Timestamp: 2006/08/24 21:51:40

Overshoot of Data 1

Pass

Limit Name: Data1_Overshoot
Current Value: 0.104166666666667

Test Criteria: < 0.15
Timestamp: 2006/08/24 21:52:19

Undershoot of Data 1

Pass

Limit Name: Data1_Undershoot
Current Value: 0.166666666666667
Test Criteria: < 0.25
Timestamp: 2006/08/24 21:52:19

Overshoot of Data 2

Pass

Limit Name: Data2_Overshoot
Current Value: 0.094736842105263
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:52:37

Undershoot of Data 2

Pass

Limit Name: Data2_Undershoot
Current Value: 0.147368421052632
Test Criteria: < 0.25
Timestamp: 2006/08/24 21:52:37

Overshoot of Clock

Pass

Limit Name: Clock_Overshoot
Current Value: 0.105263157894737
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:53:04

Undershoot of Clock

Pass

Limit Name: Clock_Undershoot
Current Value: 0.126315789473684
Test Criteria: < 0.25
Timestamp: 2006/08/24 21:53:04

Maximum Overshoot

Pass

Limit Name: Max_Overshoot
Current Value: 10.5263157894737
Test Criteria: < 15
Timestamp: 2006/08/24 21:53:04

Maximum Undershoot

Pass

Limit Name: Max_Undershoot
Current Value: 16.6666666666667
Test Criteria: < 25
Timestamp: 2006/08/24 21:53:04

7-6 Inter-Pair Skew

Tbit for Inter-Pair Skew Test

Pass

Limit Name: Tbit
Current Value: 4.07402536075833E-09
Test Criteria: > 0
Timestamp: 2006/08/24 21:53:29

Skew between Data 0 and Data 1

Fail

Failure Explanation: cur [27553652.247309] is not < ref [0.2] (1.37768e+010% error) keyword 0 numeric comparison failed
Limit Name: Inter_Pair_Skew_D0_D1
Current Value: 27553652.247309
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:54:32

Skew between Data 0 and Data 2

Fail

Failure Explanation: cur [27553652.247309] is not < ref [0.2] (1.37768e+010% error) keyword 0 numeric comparison failed
Limit Name: Inter_Pair_Skew_D0_D2
Current Value: 27553652.247309
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:54:49

Skew between Data 0 and Clock

Pass

Limit Name: Inter_Pair_Skew_D0_Ck
Current Value: 1.0168492610864E-03
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:55:43

Skew between Data 1 and Data 2

Pass

Limit Name: Inter_Pair_Skew_D1_D2
Current Value: 1.0168492610864E-03
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:56:11

Skew between Data 1 and Clock

Pass

Limit Name: Inter_Pair_Skew_D1_Ck
Current Value: 3.82606398074844E-02
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:56:22

Skew between Data 2 and Clock

Pass

Limit Name: Inter_Pair_Skew_D2_Ck
Current Value: 4.63158220156418E-02
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:56:37

Maximum Inter Pair Skew

Fail

Failure Explanation: cur [27553652.247309] is not < ref [0.2] (1.37768e+010% error) keyword 0 numeric comparison failed
Limit Name: Max_Inter_Pair_Skew
Current Value: 27553652.247309
Test Criteria: < 0.2
Timestamp: 2006/08/24 21:56:37

7-7 Intra-Pair Skew

Tbit for Intra-Pair Skew Test

Pass

Limit Name: Tbit
Current Value: 4.07405860656119E-09

Test Criteria: > 0
Timestamp: 2006/08/24 21:57:04

Skew between Data 0+ and Data 0-

Fail

Failure Explanation: cur [0.253065773844313] is not < ref [0.15] (68.7105% error) keyword 0 numeric comparison failed
Limit Name: Data0_Intra_Pair_Skew
Current Value: 0.253065773844313
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:58:07

Skew between Data 1+ and Data 1-

Fail

Failure Explanation: cur [0.899975621504597] is not < ref [0.15] (499.984% error) keyword 0 numeric comparison failed
Limit Name: Data1_Intra_Pair_Skew
Current Value: 0.899975621504597
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:58:47

Skew between Data 2+ and Data 2-

Pass

Limit Name: Data2_Intra_Pair_Skew
Current Value: -5.13623011044005E-02
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:59:02

Skew between Clock+ and Clock-

Fail

Failure Explanation: cur [0.932855195443608] is not < ref [0.15] (521.903% error) keyword 0 numeric comparison failed
Limit Name: Clock_Intra_Pair_Skew
Current Value: 0.932855195443608
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:59:36

Maximum Intra Pair Skew

Fail

Failure Explanation: cur [0.899975621504597] is not < ref [0.15] (499.984% error) keyword 0 numeric comparison failed
Limit Name: Max_Intra_Pair_Skew

Current Value: 0.899975621504597
Test Criteria: < 0.15
Timestamp: 2006/08/24 21:59:36

7-8 Clock duty Cycle

Tbit for Clock Duty Cycle test

Pass

Limit Name: Tbit
Current Value: 4.07405860656119E-09
Test Criteria: > 0
Timestamp: 2006/08/24 22:00:27

Minimum Clock Duty Cycle

Clock Duty Cycle

Pass

Limit Name: Clock_Duty_Cycle
Current Value: 49.9050478709489
Test Criteria: 40 < n < 60
Timestamp: 2006/08/24 22:00:27

Maximum Clock Duty Cycle

Clock Duty Cycle

Pass

Limit Name: Clock_Duty_Cycle
Current Value: 50.147621387623
Test Criteria: 40 < n < 60
Timestamp: 2006/08/24 22:00:27

7-9 Clock Jitter

Tbit for Clock Jitter Test

Pass

Limit Name: Tbit
Current Value: 4.0740946423594E-09
Test Criteria: > 0
Timestamp: 2006/08/24 22:00:36

Clock Jitter Value

Pass

Limit Name: Clock_Jitter

Current Value: 0.06872692575395
Test Criteria: < 0.25
Timestamp: 2006/08/24 22:00:49

Clock Jitter Histogram

Timestamp: 08/24/200622:00:52

7-10 Data Eye Diagram

--- End of report ---

HDMI Test Results Source DUT

Overall result: Fail

DUT:
Limits in use: Default
Scope SN: LCRY0401N00813
Scope Name: LCRY0401N00813
Operator:
Computer: LCRY0401N00813
Time of test: 08/25/2006 12:31:46
Temperature: 0.000000? C

Summary Table

ID	Pass/Fail	Comment
7-2 TMDS-VL		
7-4 TMDS-Trise, Tfall		_____Trise_____Tfall_____
7-5 TMDS-Over/Undershoot		
7-6 TMDS-Inter_Pair Skew		
7-7 TMDS-Intra_Pair Skew		
7-8 TMDS-Clock Duty Cycle		
7-9 TMDS-Clock Jitter		
7-10 TMDS-Data Eye Diagram		

Details

7-10 Data Eye Diagram

Tbit for Data Eye Test for Data 0

Pass

Limit Name: Tbit
Current Value: 1.34815657634234E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:32:32

Eye Violation of Data 0

Pass

Limit Name: Data0_Eye_Violation
Current Value: 0
Test Criteria: <= 1
Timestamp: 2006/08/25 12:32:41

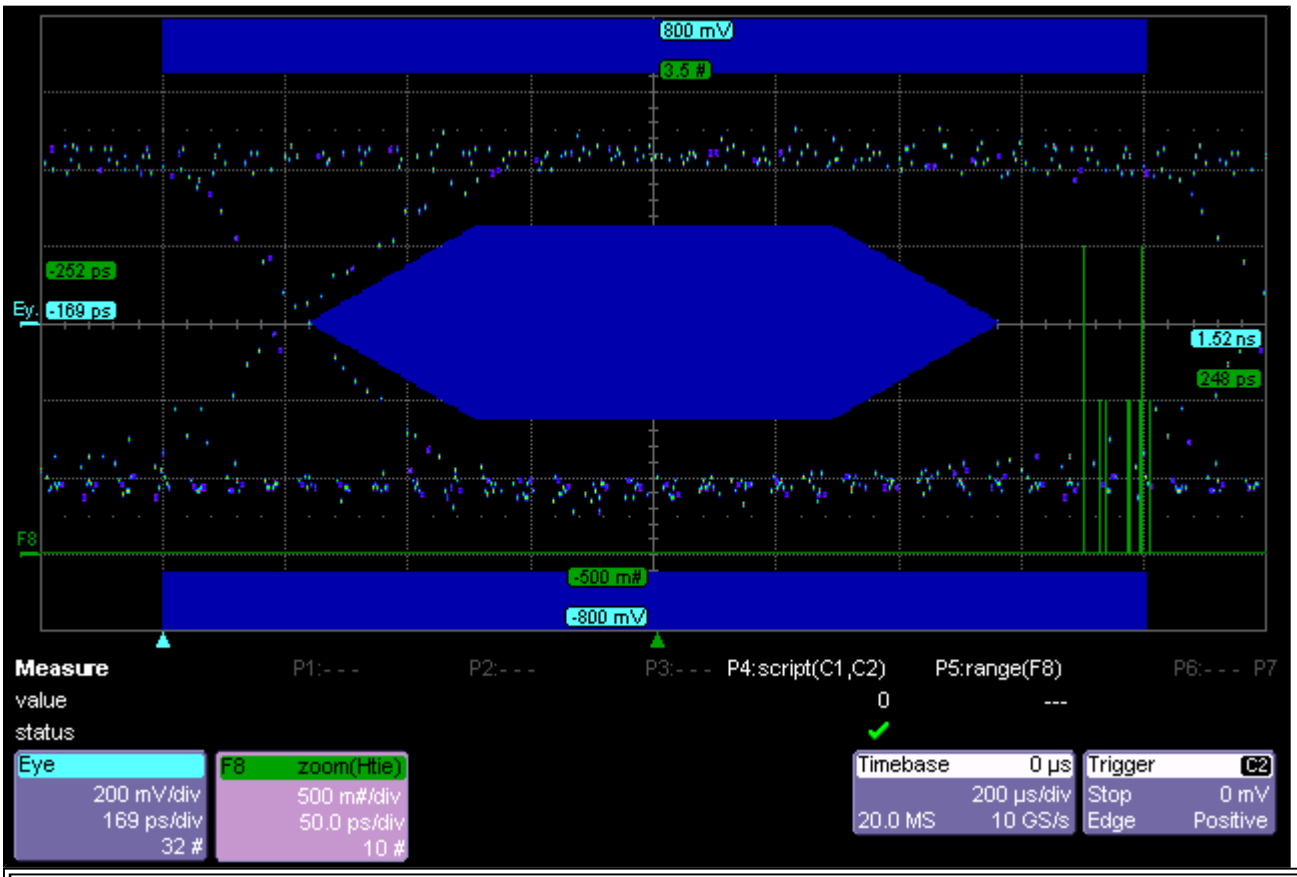
Data Jitter of Data 0

Pass

Limit Name: Data0_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:32:41

Data Eye Diagram of Data 0

Timestamp: 08/25/200612:32:46



Tbit for Data Eye Test for Data 0

Pass

Limit Name: Tbit
Current Value: 1.34813858203325E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:33:23

Eye Violation of Data 1

Pass

Limit Name: Data1_Eye_Violation
Current Value: 0
Test Criteria: <= 1
Timestamp: 2006/08/25 12:33:34

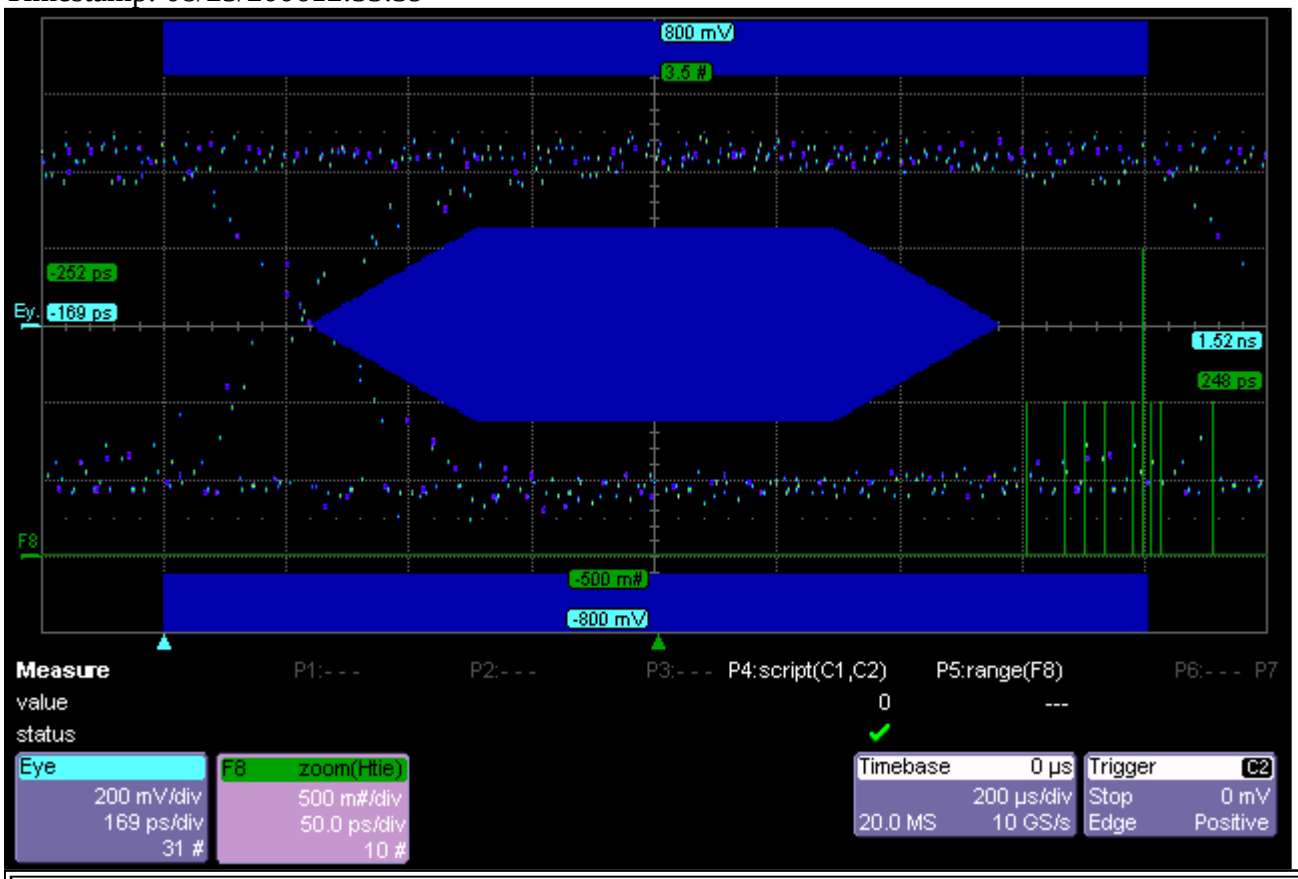
Data Jitter of Data 1

Pass

Limit Name: Data1_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:33:34

Data Eye Diagram of Data 1

Timestamp: 08/25/200612:33:39



Tbit for Data Eye Test for Data 2

Pass

Limit Name: Tbit
Current Value: 1.34815976911022E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:34:18

Eye Violation of Data 2

Pass

Limit Name: Data2_Eye_Violation
Current Value: 0
Test Criteria: <= 1
Timestamp: 2006/08/25 12:34:27

Data Jitter of Data 2

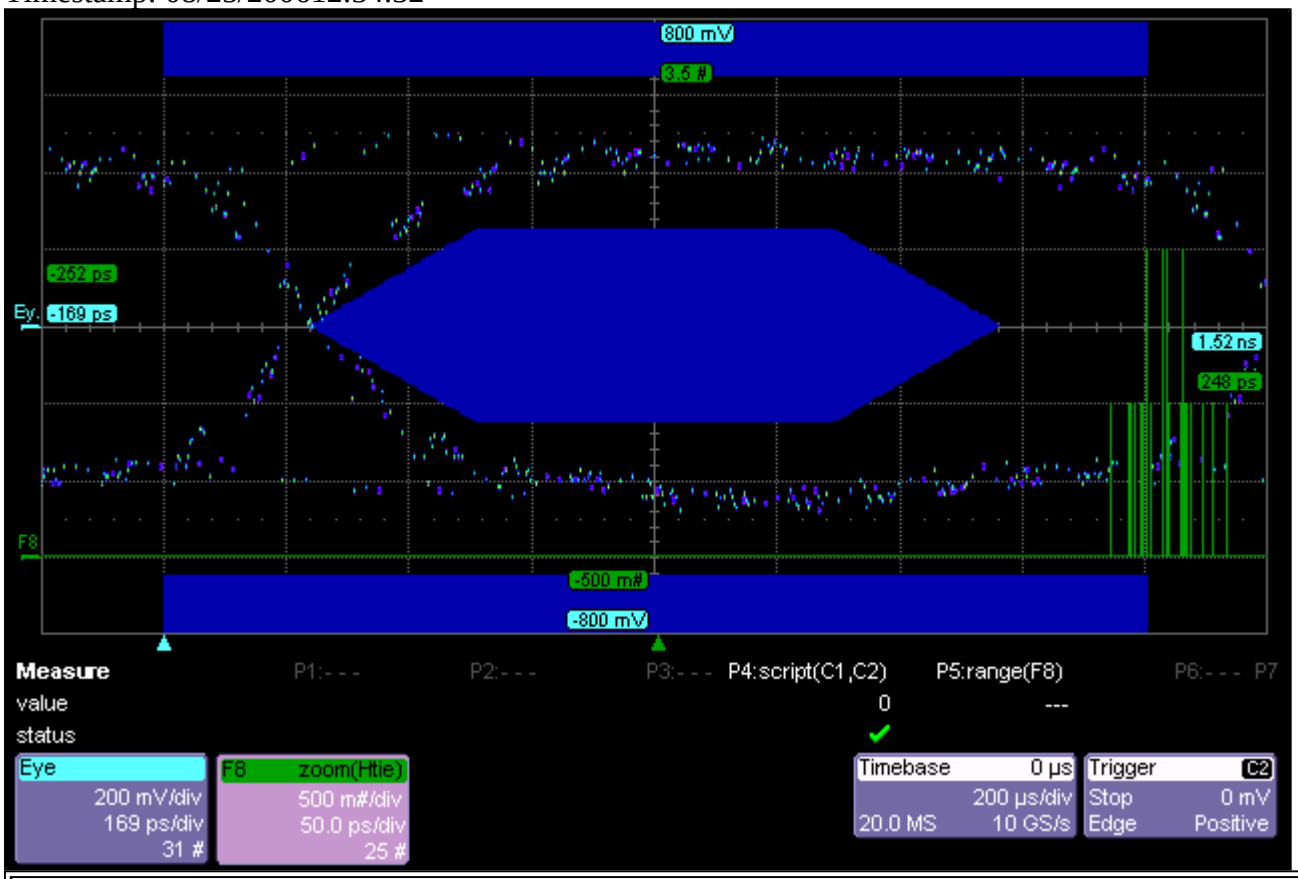
Pass

Limit Name: Data2_Jitter

Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:34:27

Data Eye Diagram of Data 2

Timestamp: 08/25/200612:34:32



Tbit for Data Eye Test for Data 0

Pass

Limit Name: Tbit
Current Value: 1.34815569886723E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:35:37

Eye Violation of Data 0

Pass

Limit Name: Data0_Eye_Violation
Current Value: 0
Test Criteria: <= 1
Timestamp: 2006/08/25 12:35:47

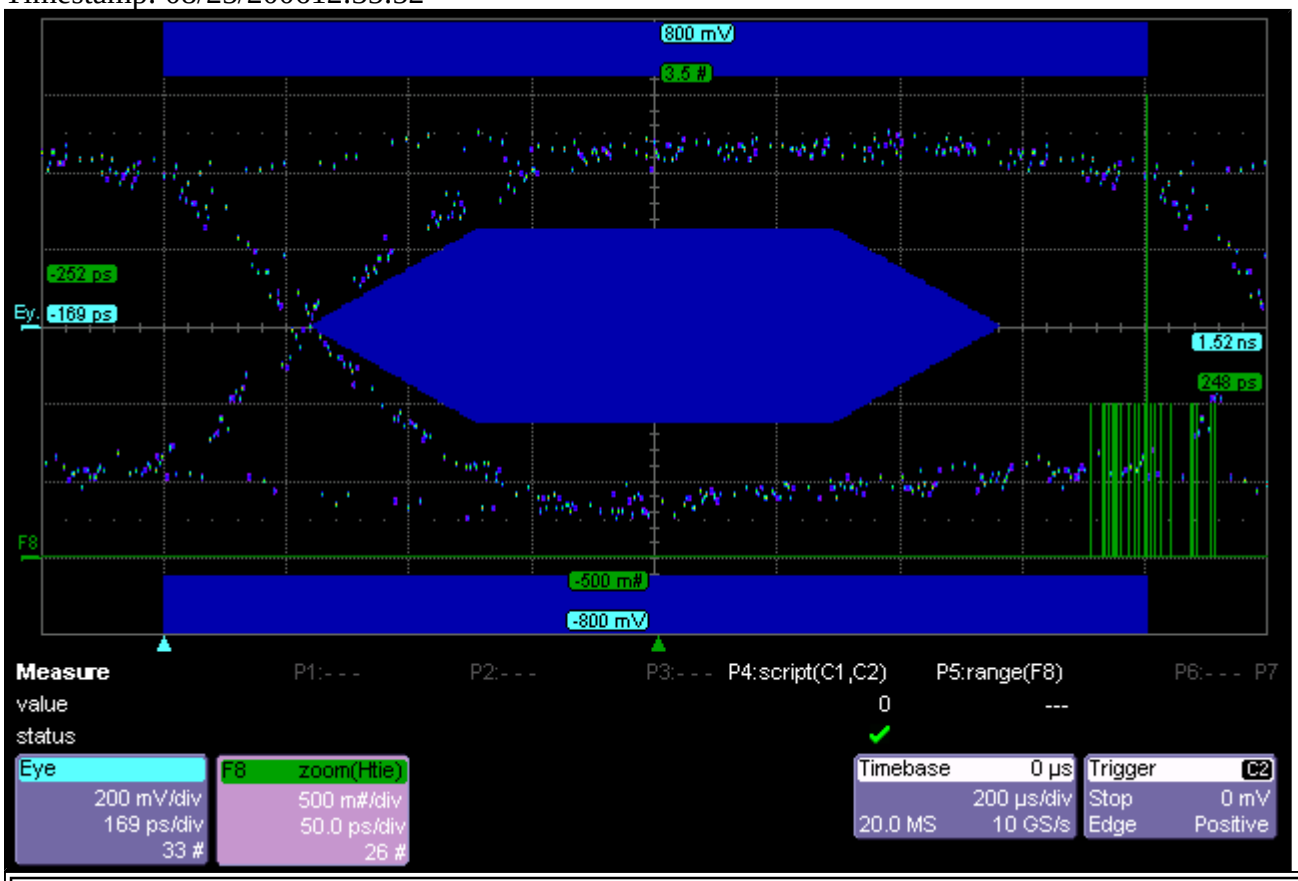
Data Jitter of Data 0

Pass

Limit Name: Data0_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:35:47

Data Eye Diagram of Data 0

Timestamp: 08/25/200612:35:52



Tbit for Data Eye Test for Data 0

Pass

Limit Name: Tbit
Current Value: 1.34819669277498E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:36:22

Eye Violation of Data 1

Pass

Limit Name: Data1_Eye_Violation
Current Value: 0
Test Criteria: <= 1

Timestamp: 2006/08/25 12:36:33

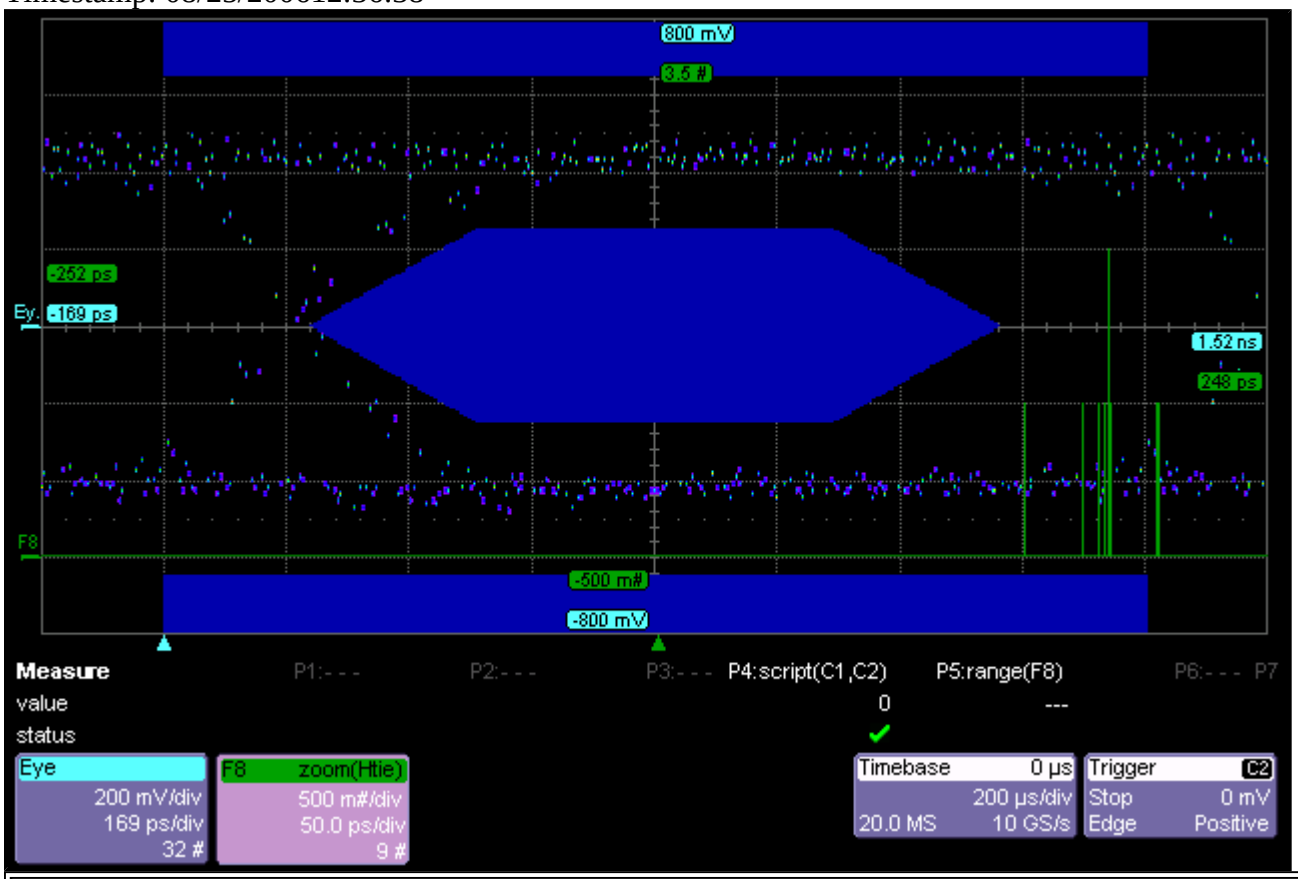
Data Jitter of Data 1

Pass

Limit Name: Data1_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:36:33

Data Eye Diagram of Data 1

Timestamp: 08/25/200612:36:38



Tbit for Data Eye Test for Data 2

Pass

Limit Name: Tbit
Current Value: 1.34815987494239E-09
Test Criteria: > 0
Timestamp: 2006/08/25 12:37:10

Eye Violation of Data 2

Fail

Failure Explanation: cur [2] is not <= ref [1] (100% error) keyword 0 numeric comparison failed
Limit Name: Data2_Eye_Violation
Current Value: 2
Test Criteria: <= 1
Timestamp: 2006/08/25 12:37:20

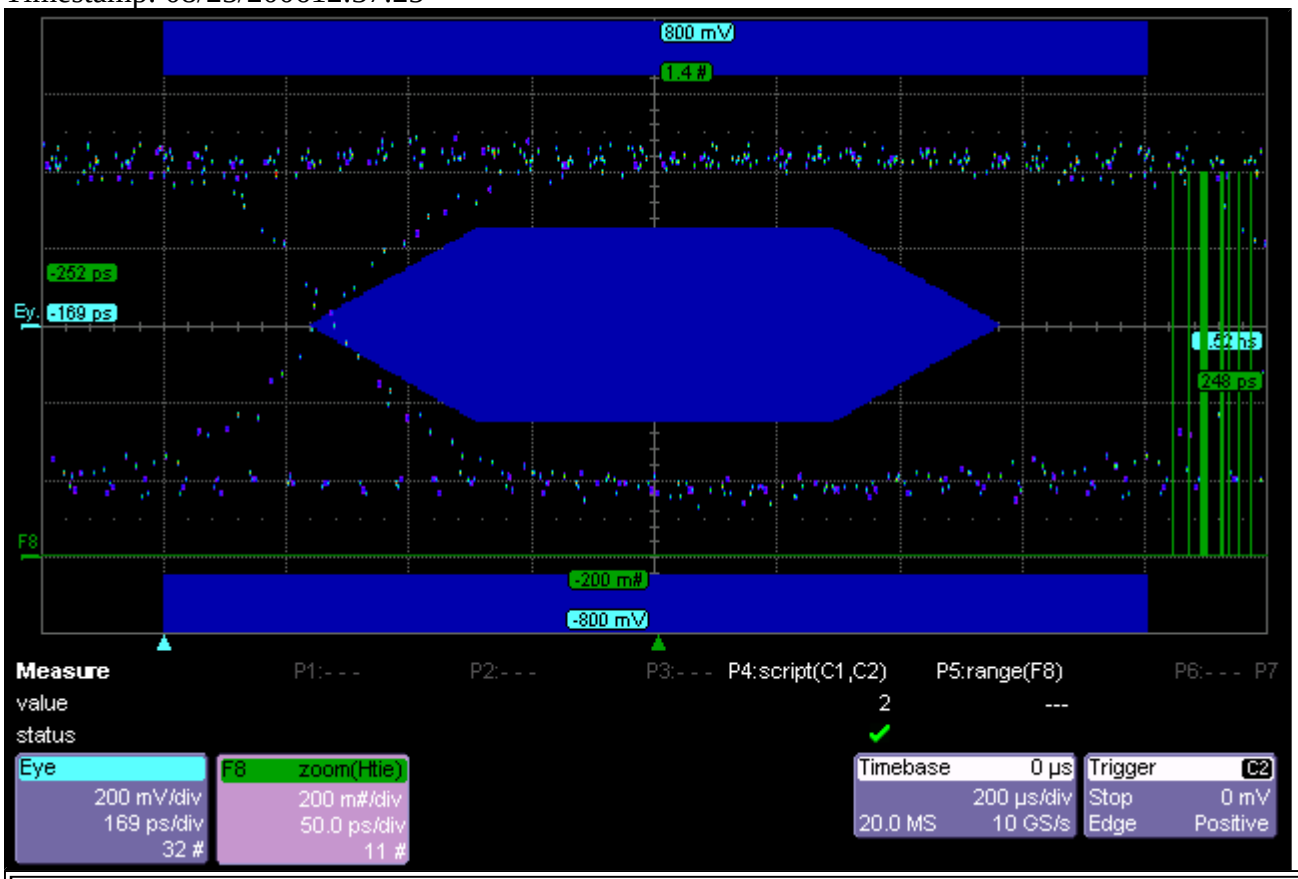
Data Jitter of Data 2

Pass

Limit Name: Data2_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:37:20

Data Eye Diagram of Data 2

Timestamp: 08/25/200612:37:25



Tbit for Data Eye Test for Data 2

Pass

Limit Name: Tbit
Current Value: 1.34814207961588E-09

Test Criteria: > 0
Timestamp: 2006/08/25 12:37:56

Eye Violation of Data 2

Pass

Limit Name: Data2_Eye_Violation
Current Value: 0
Test Criteria: <= 1
Timestamp: 2006/08/25 12:38:04

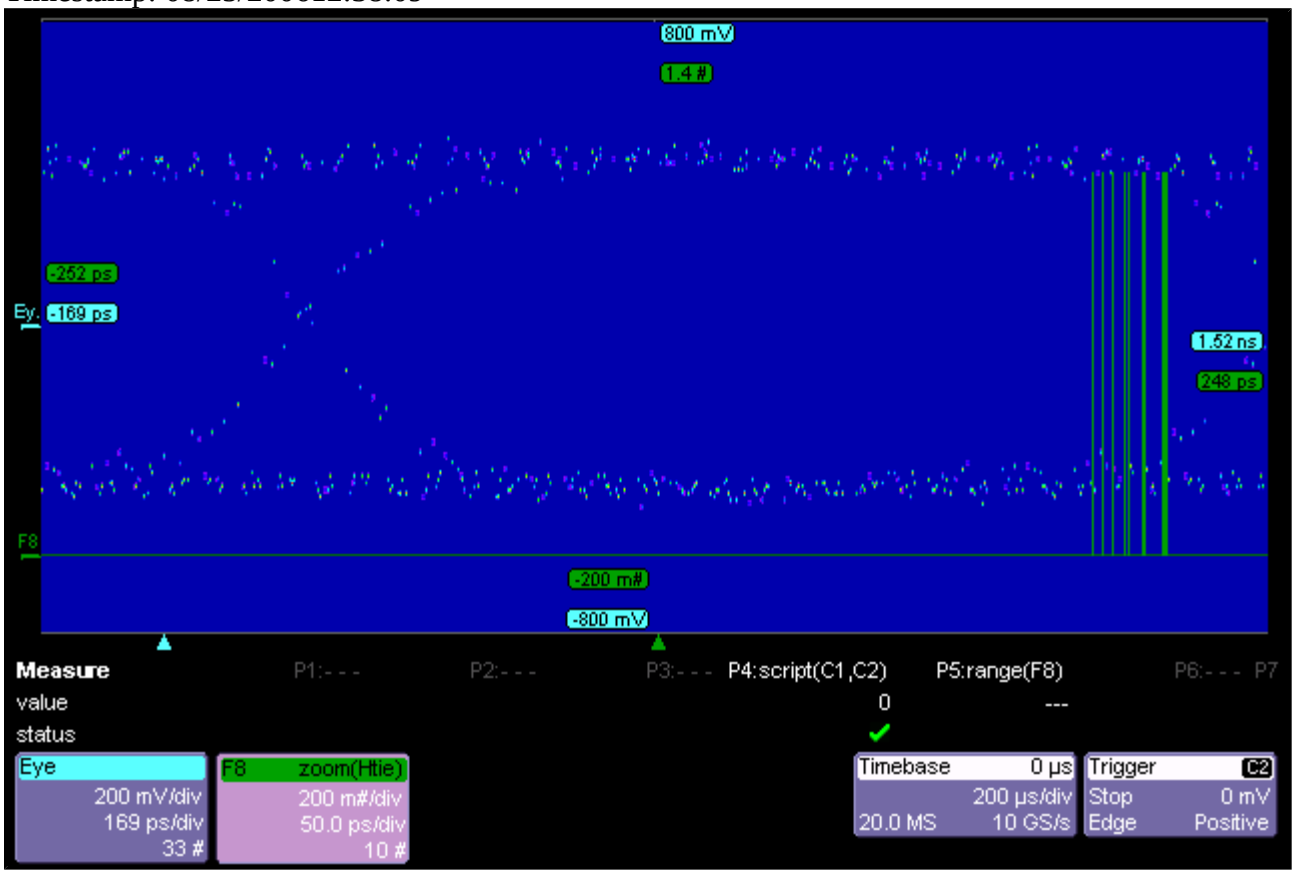
Data Jitter of Data 2

Pass

Limit Name: Data2_Jitter
Current Value: 0
Test Criteria: < 0.3
Timestamp: 2006/08/25 12:38:04

Data Eye Diagram of Data 2

Timestamp: 08/25/200612:38:09



--- End of report ---